



it's about what's next.®

How to build an IC Company

Presentation to Stanford University EE380 – October 2020



Do you have an idea worth pursuing?



Do You Have a product worthy of building a company?

Identify

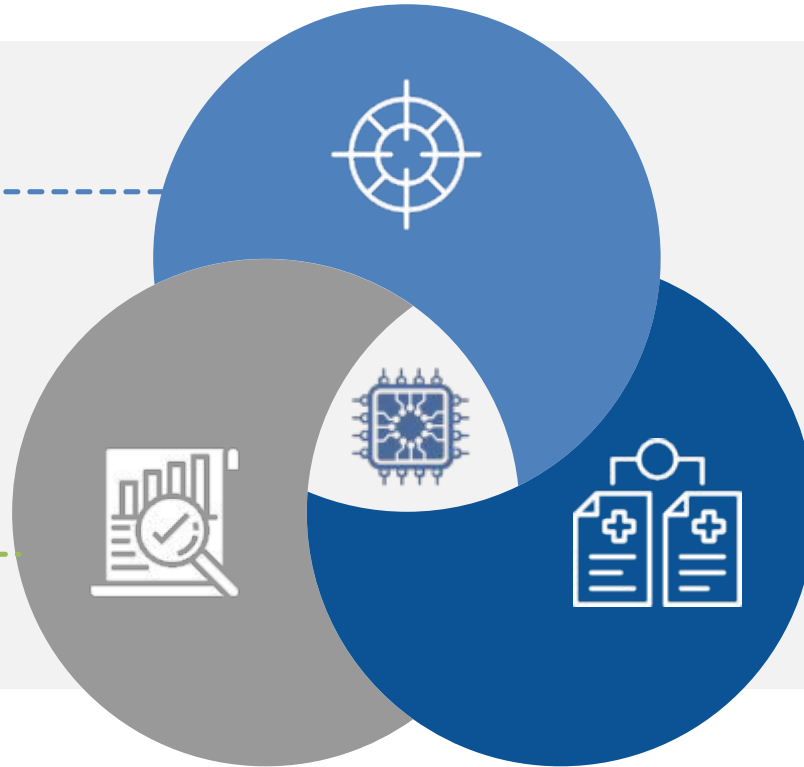
First lay out the target customer needs
Then show your solution meets each of these needs precisely

Justify

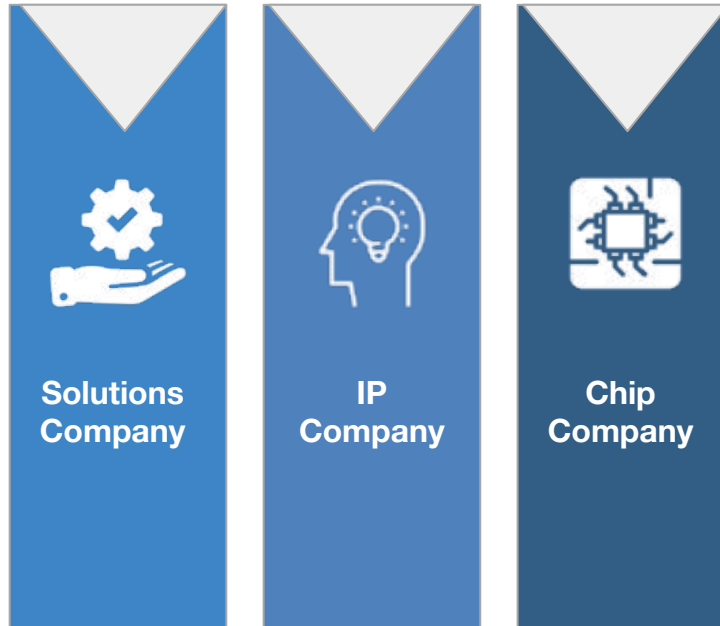
Are there enough customers in that profile to justify building a business?

Assess

Which companies are already selling something to your target customers, who might want to add another product to their portfolio?



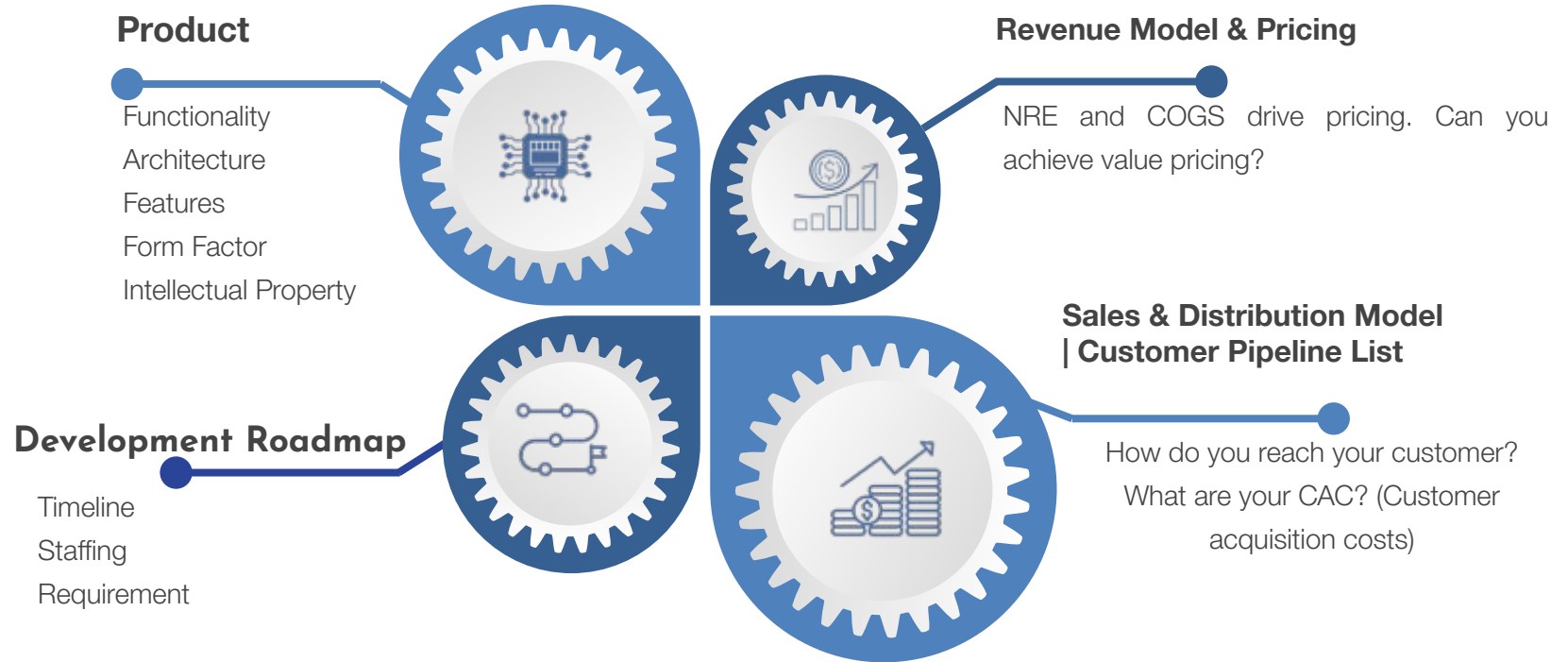
What kind of company would you like to build?



Create a solutions companies that needs a new IC

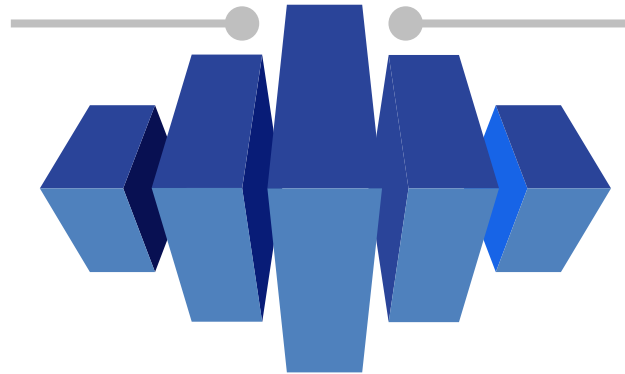
Business plan/Go To Market

These items will drive your costs and how much money you need to raise.



Why now?

Will the market be ready?

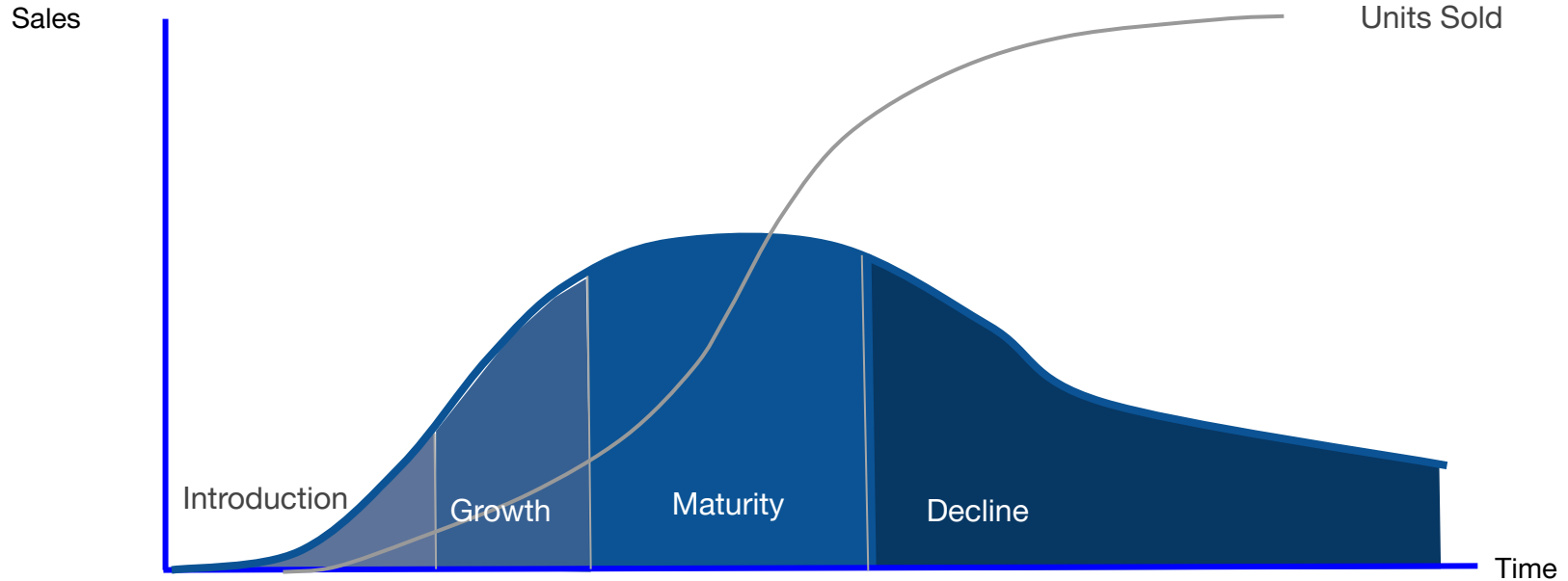


Can your product be developed in time for the market?

IC Development can take multiple years, will you hit the market window?

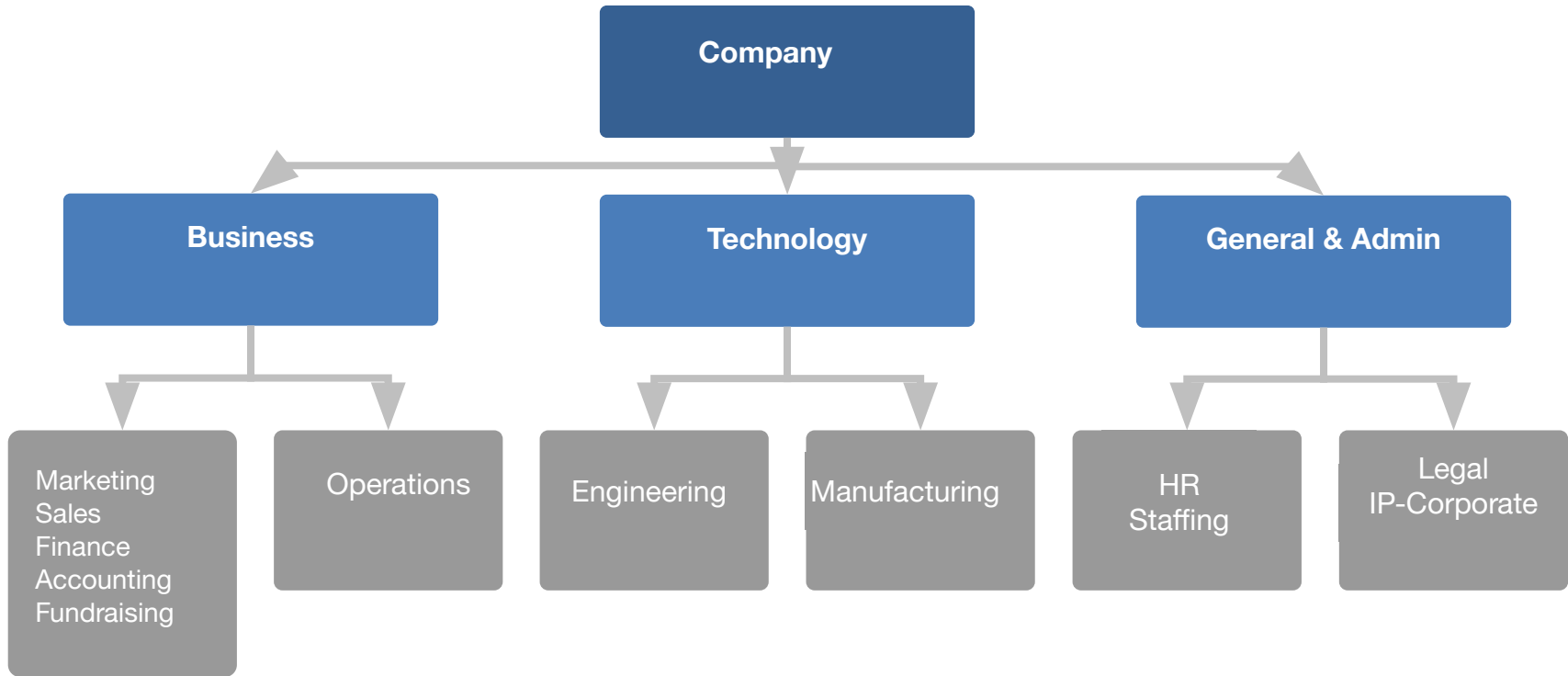
Market timing

Can you hit the window of opportunity?



Building a company takes the right team

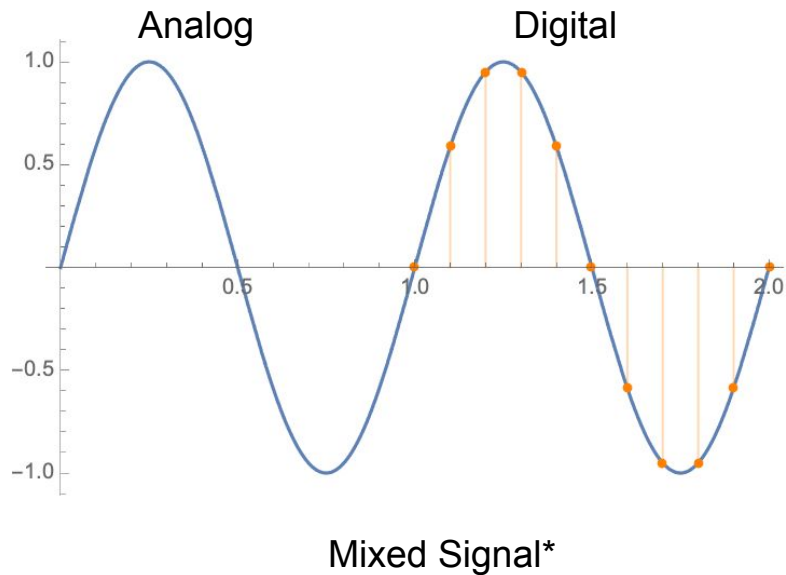
Investors want to know you have the knowledge base for running a company not just building a product



Path to Product For building an IC

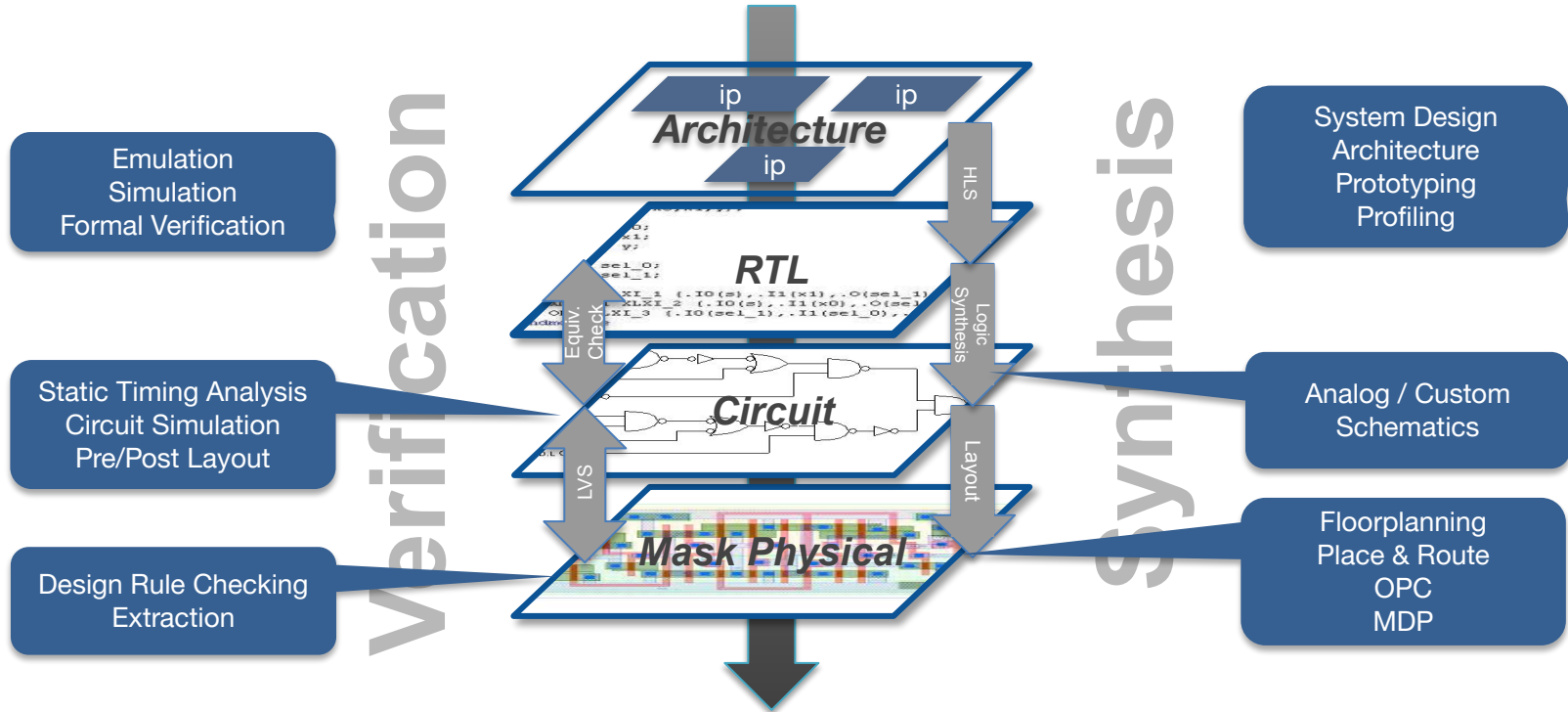


Types of ICs



* <https://semiengineering.com/increase-in-analog-problems/>

IC Design



Numerous* EDA Tools Required

Verification

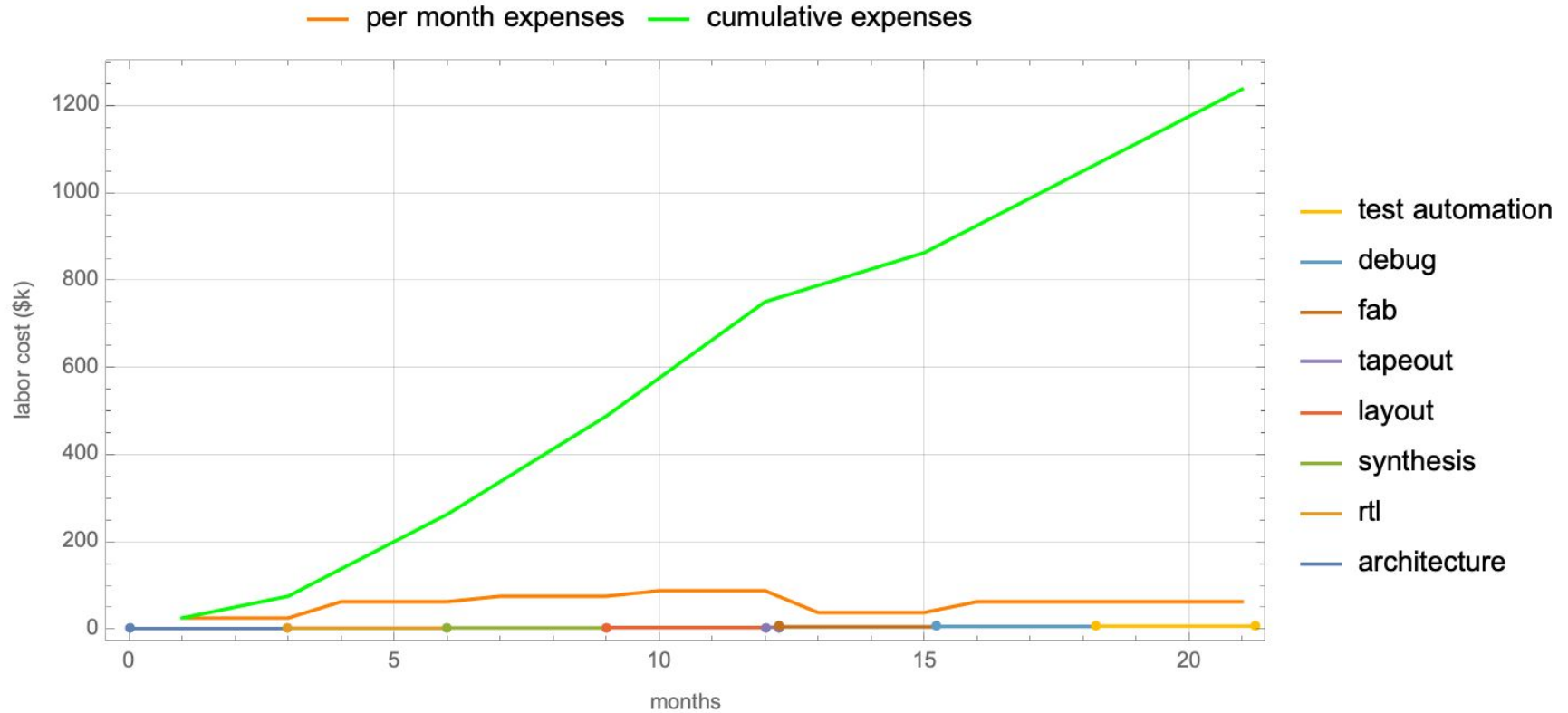
- Emulation
- System Simulation
- Logic Simulation
- Circuit Simulation
- Static Timing Analysis
- Power Analysis
- Design Rule Check
- Parasitic Extraction
- ...

Synthesis

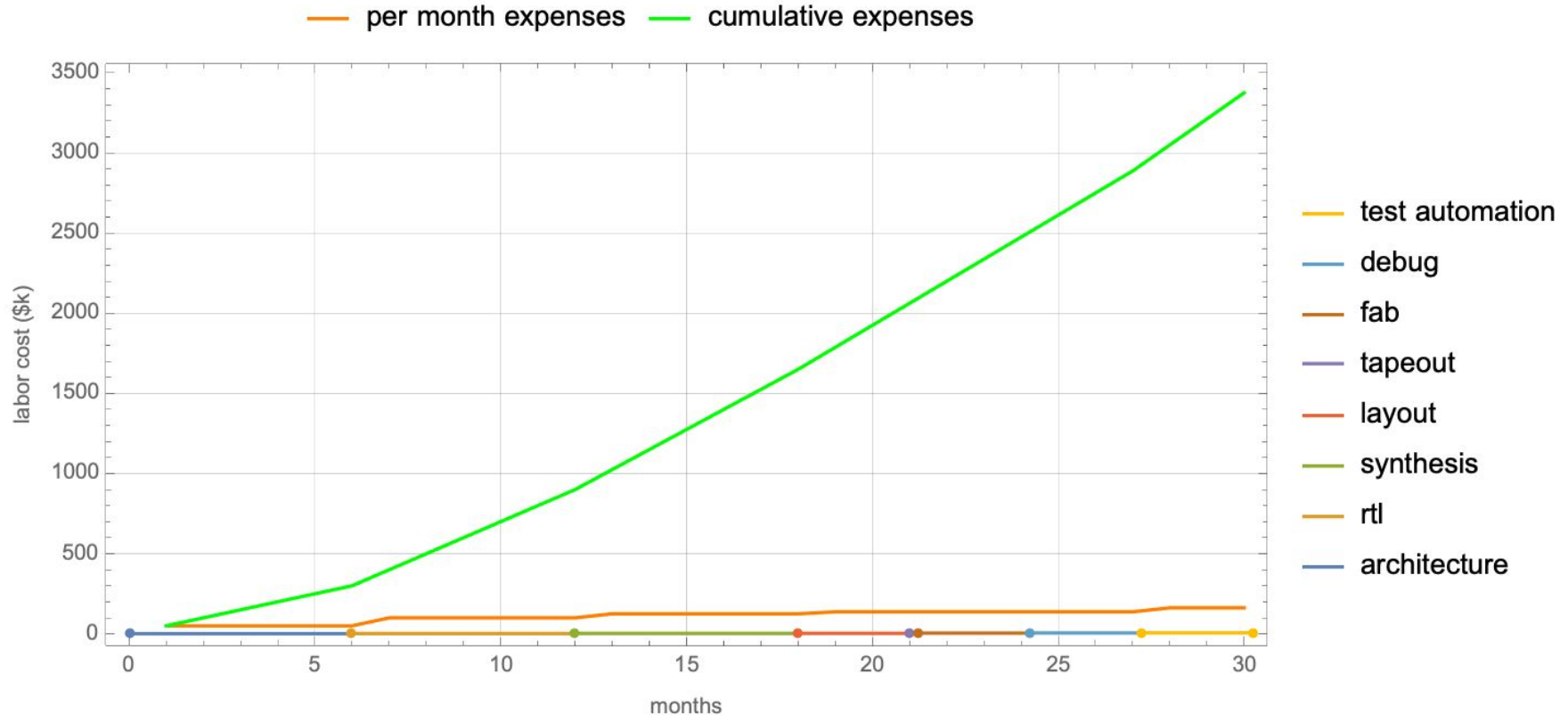
- High Level Synthesis
- Floorplanning
- Logic Synthesis
- Technology mapping
- Placement
- Routing
- Optical Proximity Correction
- Mask Data Preparation
- ...

* ESDA Lists over 30 categories of EDA Tools

Scenario 1: Minimalist

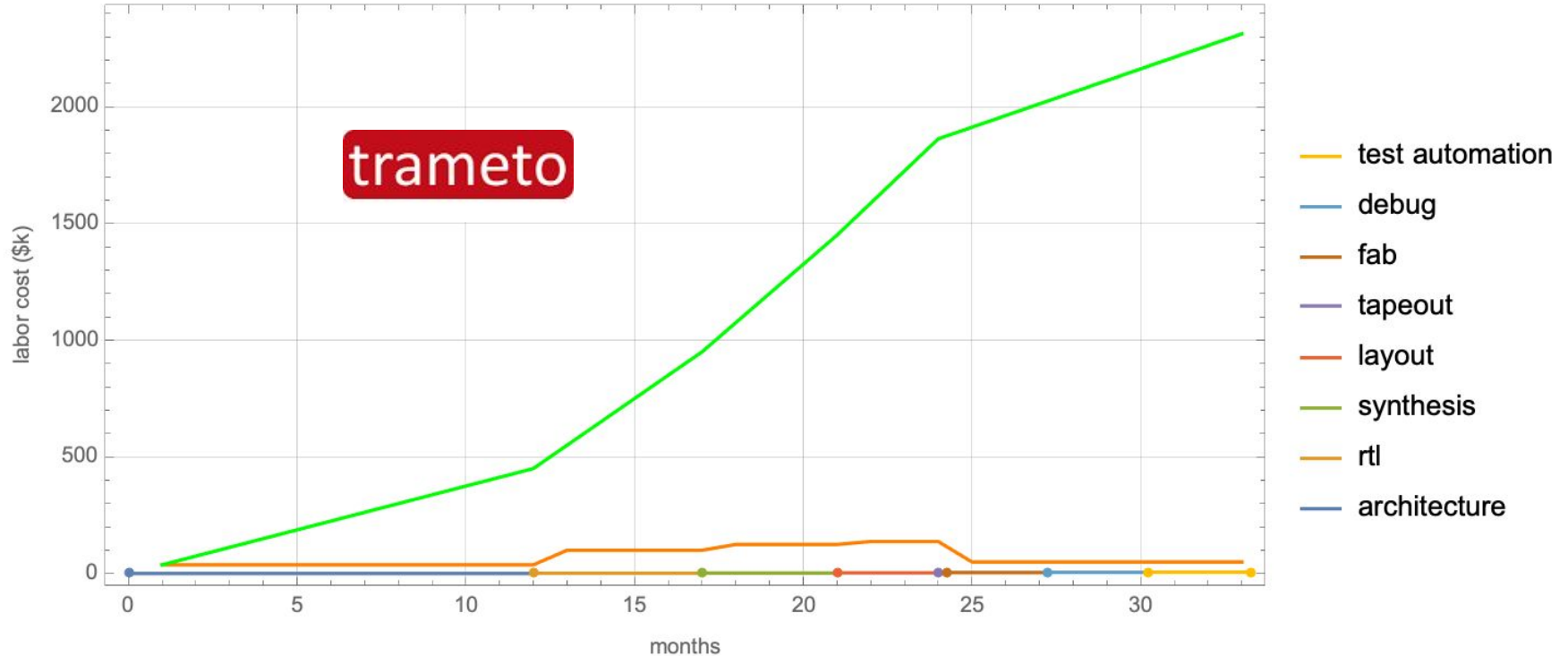


Scenario 2: Longer Time, Accumulating Staff

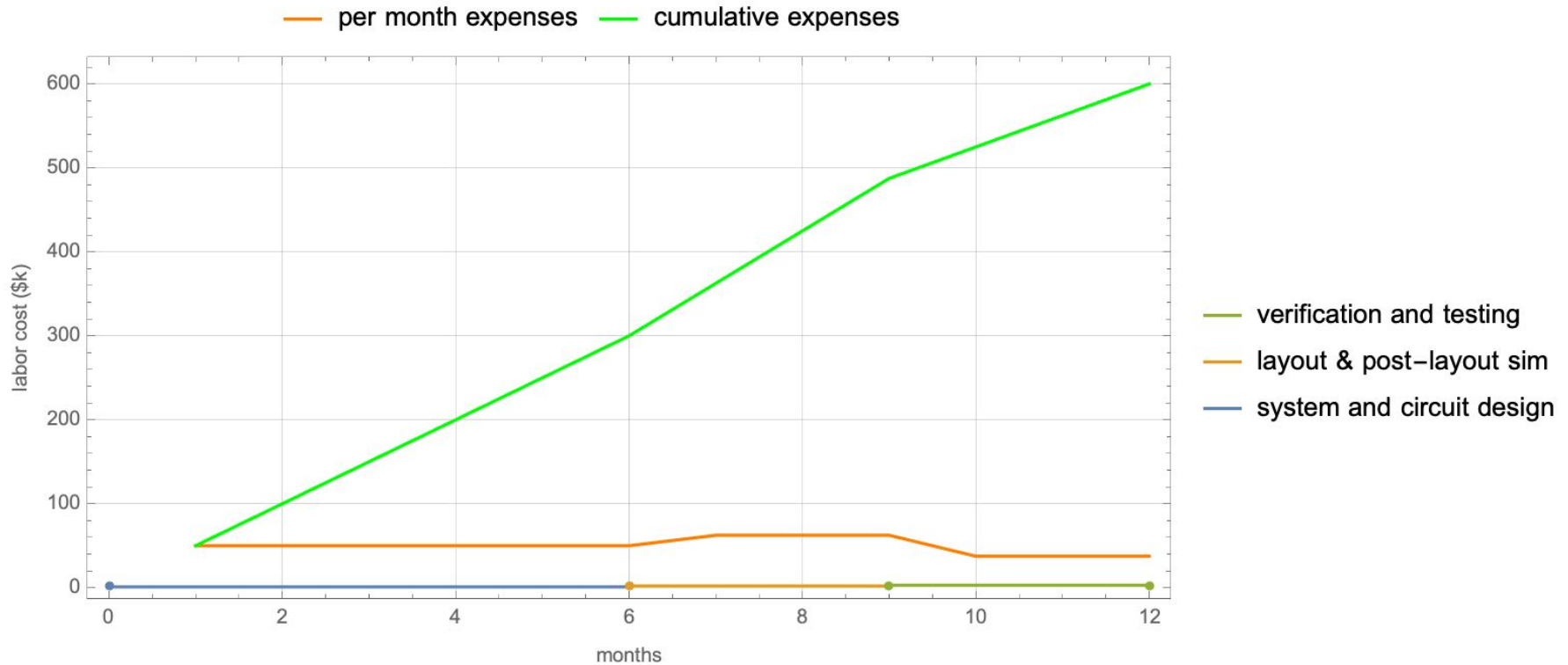


Example 1: Mixed Signal

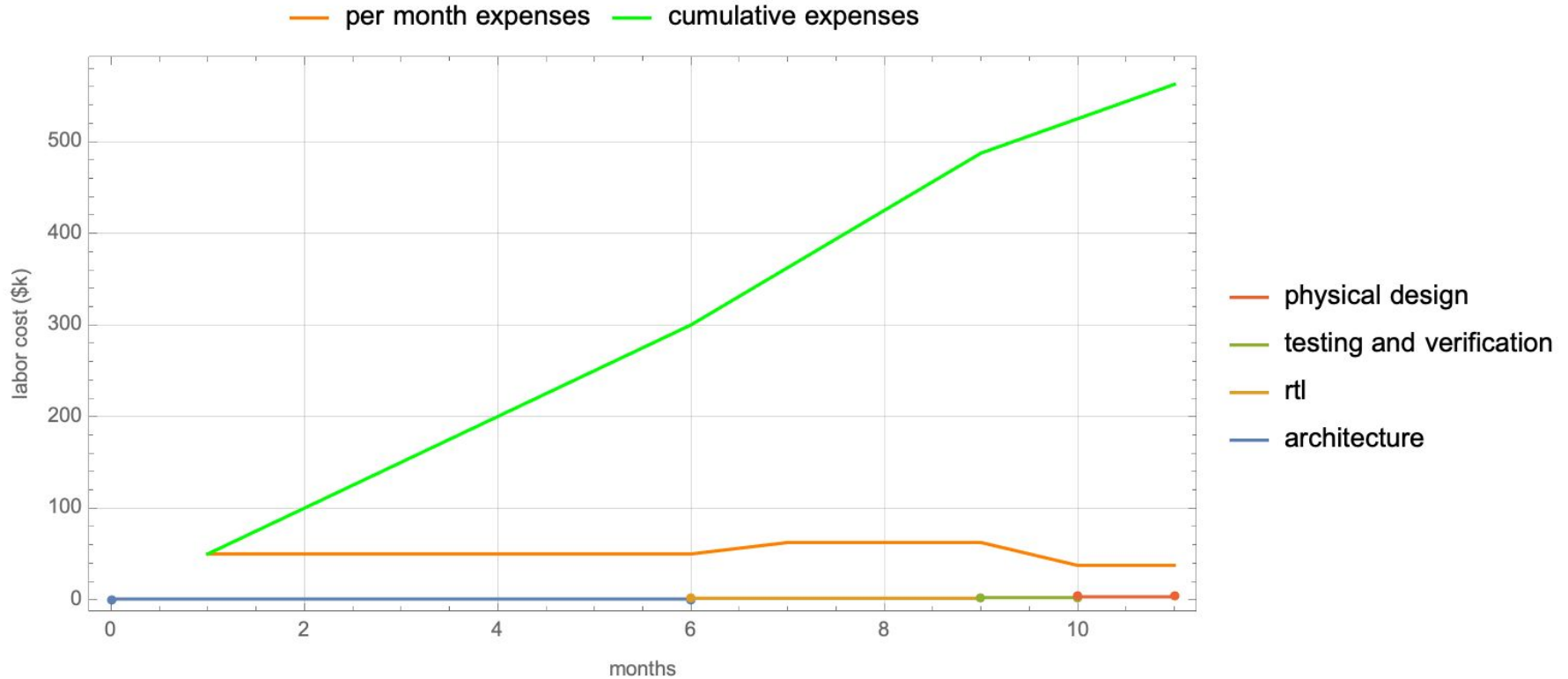
per month expenses cumulative expenses



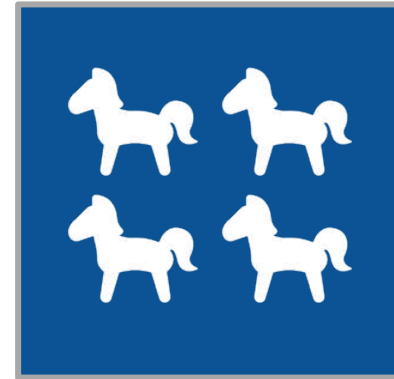
Example 2: Mostly Analog



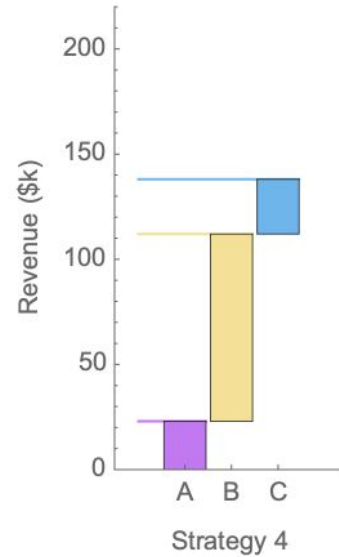
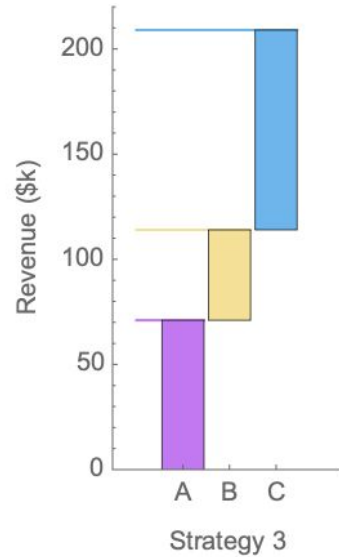
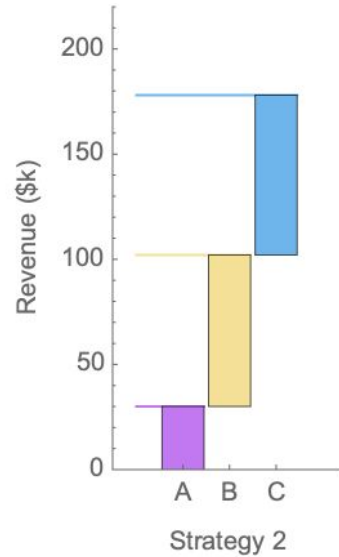
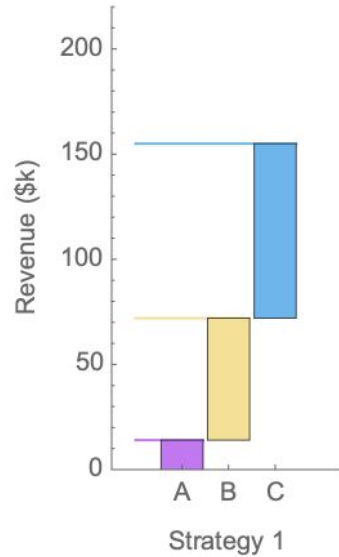
Example 3: Digital



Maximizing Chance For Success



Product Mix Example

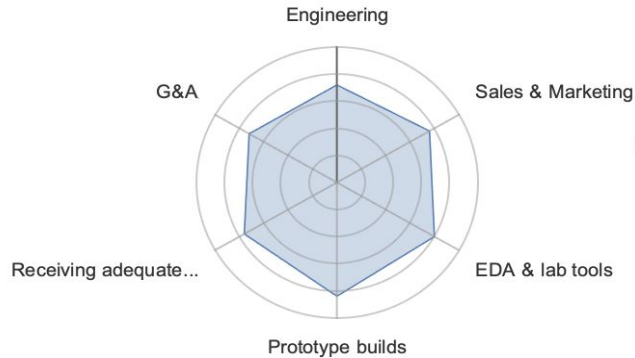


- Product A
- Product B
- Product C

What Do Semiconductor Startups Struggle With?

“It’s difficult to raise money for chip startups with Powerpoint or even simulations”

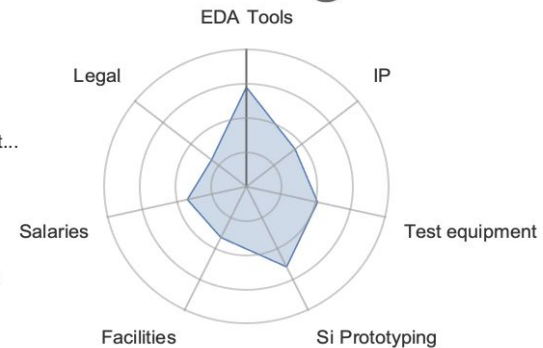
Issues



Expenses



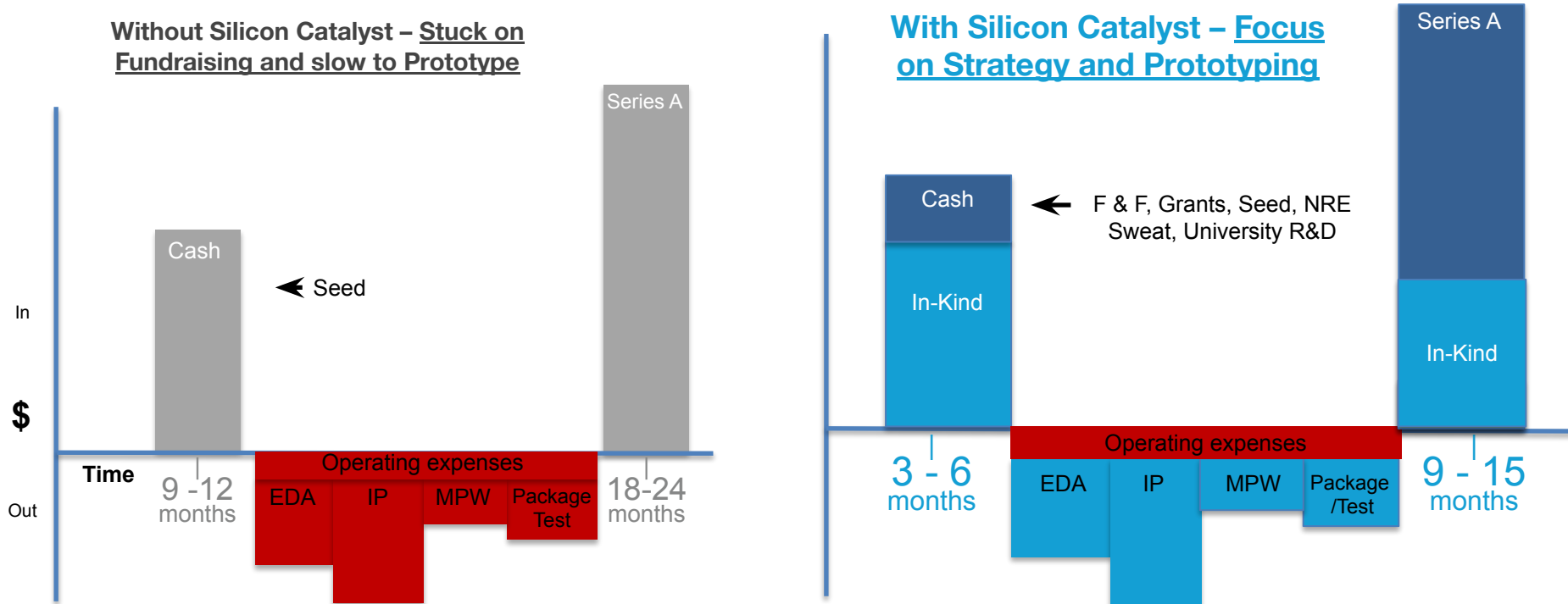
Challenges



Reduces the Seed Investment and the Time to Prototype



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Silicon Catalyst receives Common Equity in exchange for incubation

Design

SYNOPSYS
Silicon to Software®

Mentor
A Siemens Business

MathWorks

KEYSIGHT
TECHNOLOGIES

ANSYS

COVENTOR
A Lam Research Company

SILVACO

SoftMEMS
Bringing MEMS to the Mainstream

lumerical

ICmanage

S2C
FPGA PROTOTYPING SOLUTIONS

efabless

IP

arm

SYNOPSYS
Silicon to Software®

siFive

COVENTOR
A Lam Research Company

CERTUS
semiconductor

lumerical
An ANSYS Business

INTRINSIX

SILVACO

LATTICE
SEMICONDUCTOR

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dxcorr

Des. Service

INTRINSIX

umec

siFive

AMRITZGERALD

CODEMAYA

LATTICE
SEMICONDUCTOR

TESSOLVE
A Hero Electronix Ventures

dxcorr

In-Kind Partners

Foundry

tsmc

life.augmented

TSI
SEMICONDUCTORS

umec

LATTICE
SEMICONDUCTOR¹

PDF/SOLUTIONS²

Test/backend

ADVANTEST

KEYSIGHT
TECHNOLOGIES

EAG
LABORATORIES
A EUROFINIS COMPANY

AUTODESK

PDF/SOLUTIONS

silitronics
Vertically Integrated Building Block Solutions

umec

siFive

INTRINSIX

TESSOLVE
A Hero Electronix Ventures

Business

amazon
web services

rescale

O'Melveny

svb
Silicon Valley Bank

hrfm | heslin rothenberg
farley mesiti
ALL IP. ALL THE TIME.

myStartUp
As much CFO as you need

CODEMAYA

Harvest
Management
Partners LLC.

SalesDev
GLOBAL

EHRlich GROUP
TURNING IDEAS INTO VALUE³

GKH
LAW OFFICES³



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¹ Low Volume; ² High Volume Yield Improvement; ³ Israel Only

Our startups launched from Universities



Enabling the next phase of Moore's Law through optical connectivity



Silicon Photonics on MEMS with the low cost structure of Microelectronics



Multi-scale biochemical phenotyping in limited sample volume



Analog In-memory Computing for AI



Embedded SRAM using 1T & 2T cells in standard foundry flow



Ultra-low energy, ultra-low power wireless communications



High-performance AMS designs for consumer medical imaging, 5G and LiDAR



THE NEXT GENERATION OF PROCESSING

Hi performance compute for AI



GHz ultrasonic for Imaging Sensing and IOT



Join us in driving innovation!



it's about what's next.®

internet of things
IoT
SILICON
CATALYST

artificial intelligence
AI
SILICON
CATALYST

wearables
W
SILICON
CATALYST

biotechnology
Bio
SILICON
CATALYST

energy
E
SILICON
CATALYST

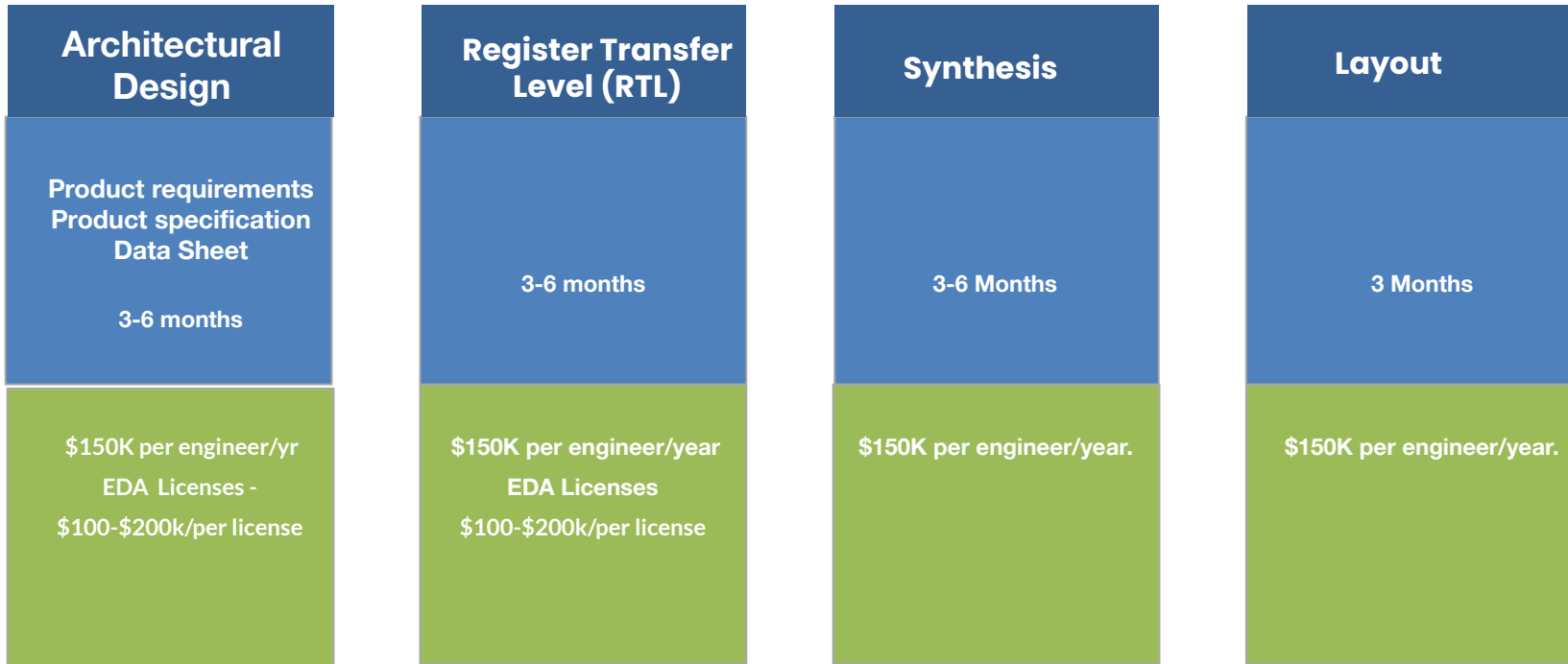
transportation
T
SILICON
CATALYST

high voltage
HV
SILICON
CATALYST

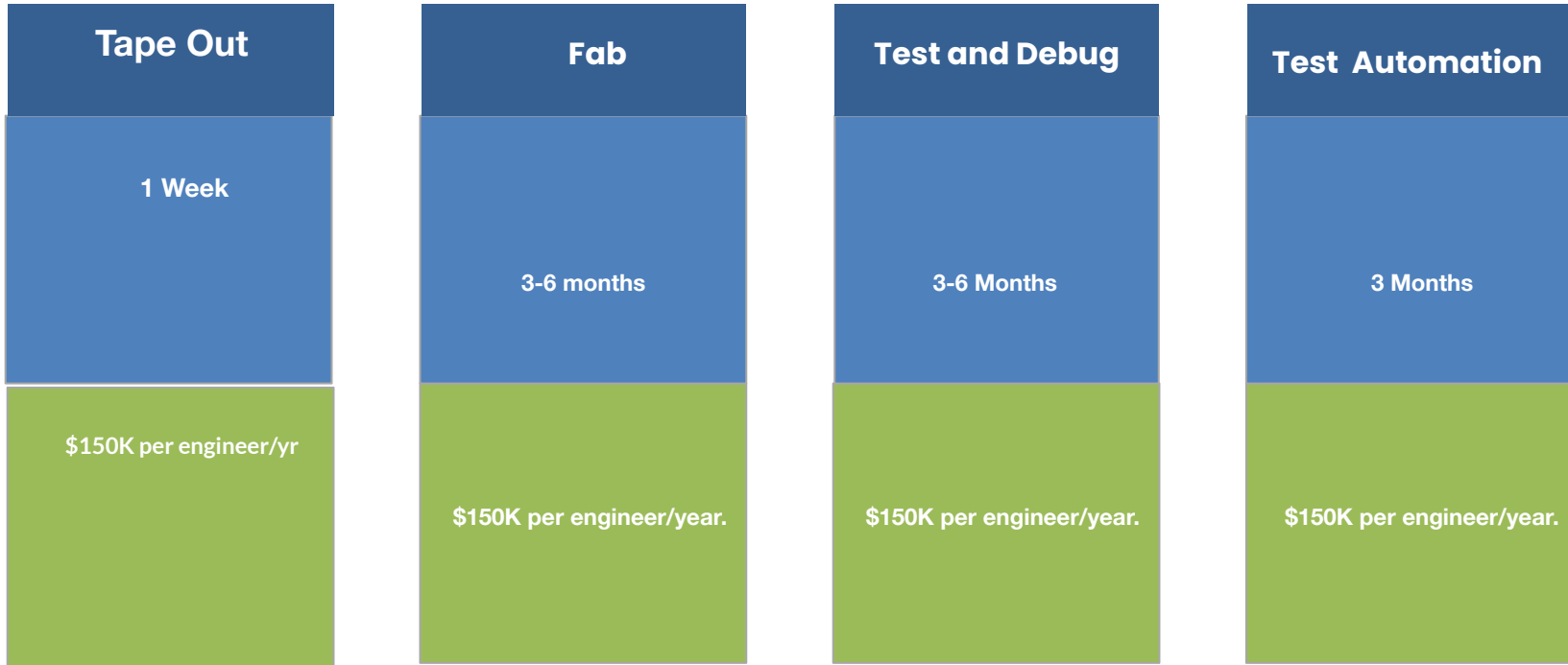


www.siliconcatalyst.com

IC Development - Time and Money



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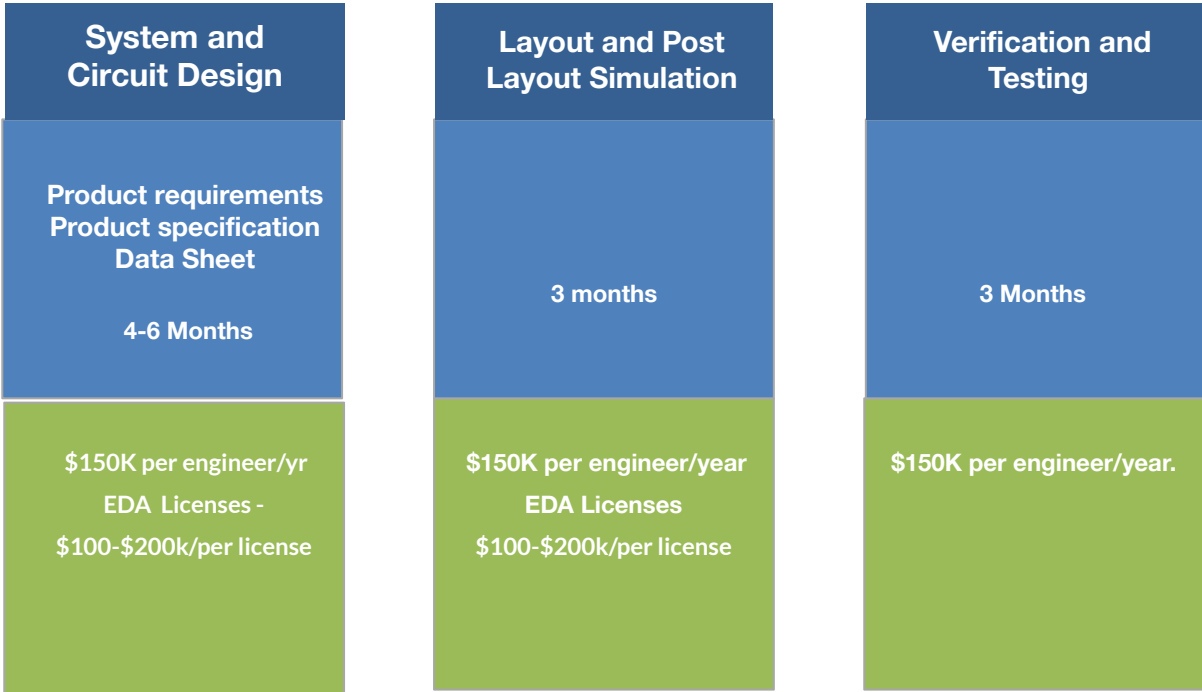
trameto



	Architectural Design	Register Transfer Level (RTL)	Synthesis	Layout
Time	Product requirements Product specification Data Sheet 10-12 Months	5 months	4 Months	3 Months
Cost	\$150K per engineer/yr EDA Licenses - \$100-\$200k/per license	\$150K per engineer/year EDA Licenses \$100-\$200k/per license	\$150K per engineer/year.	\$150K per engineer/year.

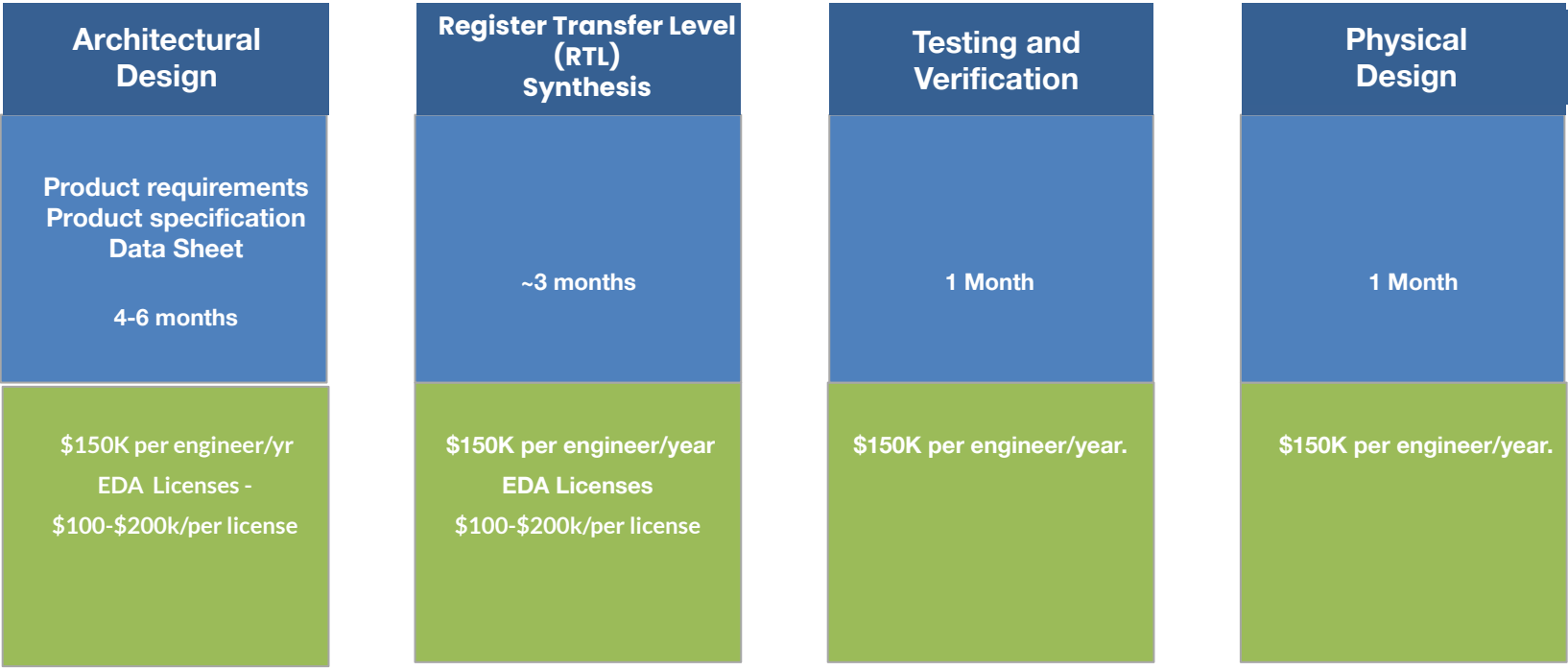
IC Development - Time and Money

Company X- Analog



IC Development - Time and Money

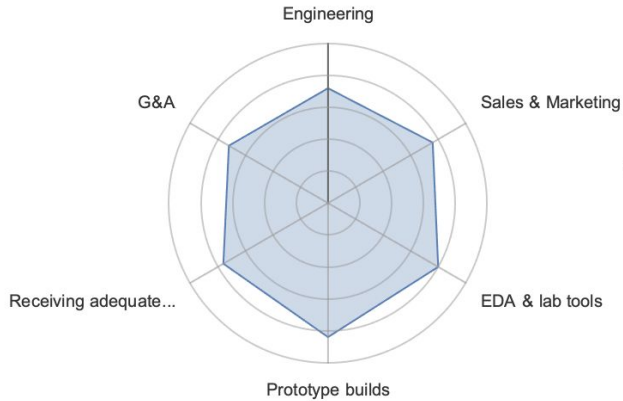
Company X- Digital



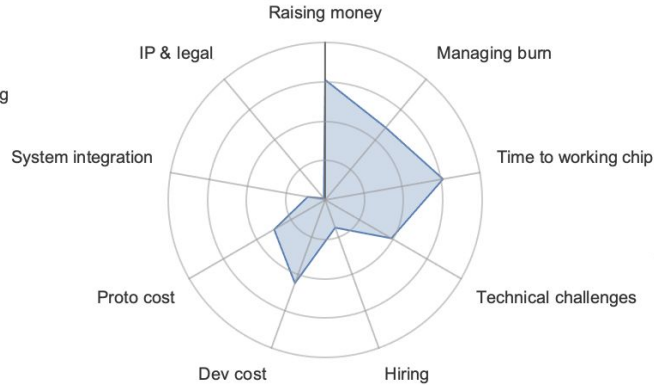
What Do Semiconductor Startups Struggle With?

“It’s difficult to raise money for chip startups with Powerpoint or even simulations”

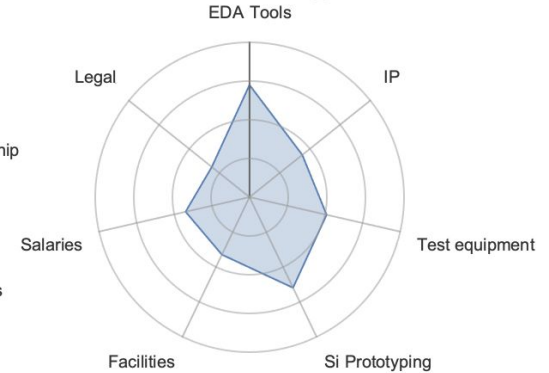
Issues



Expenses



Challenges



Source: Silicon Catalyst, 15 startups surveyed in 2014

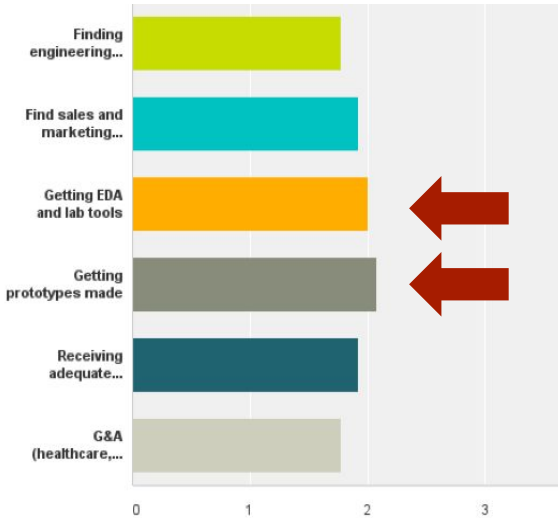
Maximizing Chance For Success



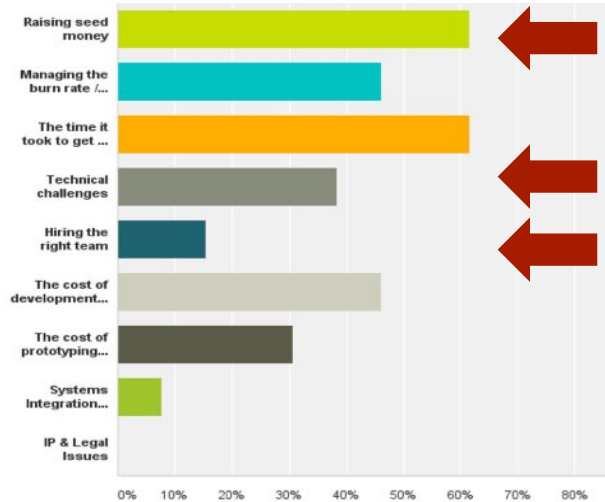
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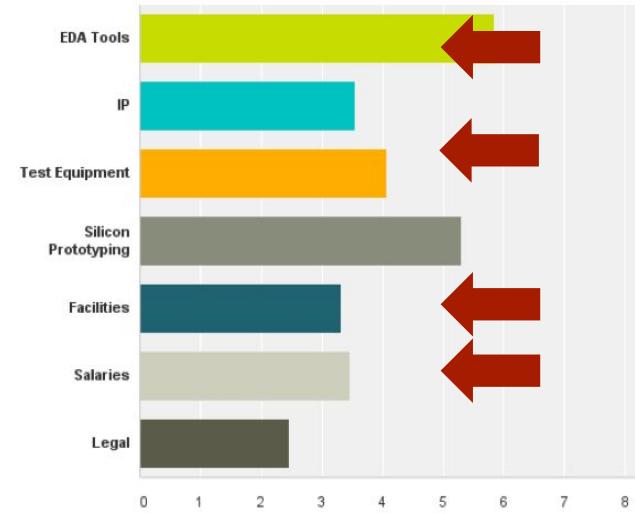
Rank Issues



Rank Expenses



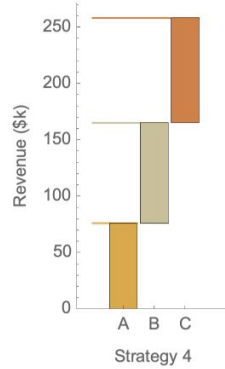
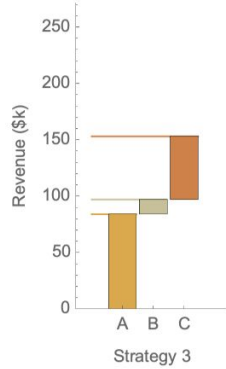
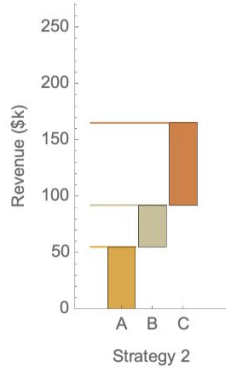
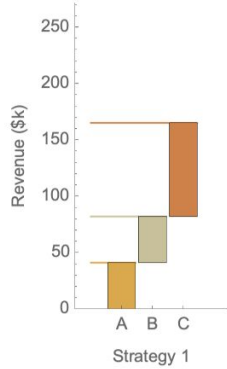
Top Challenges



Time, EDA, Prototypes, Test, \$'s ←

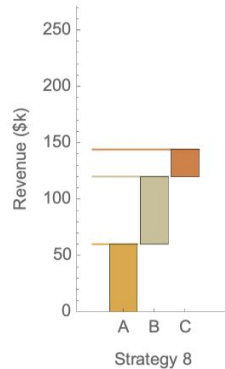
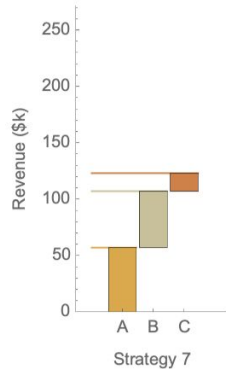
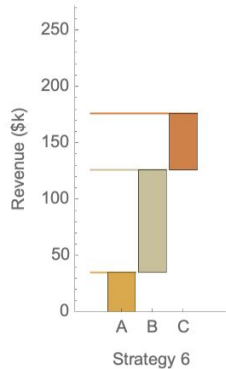
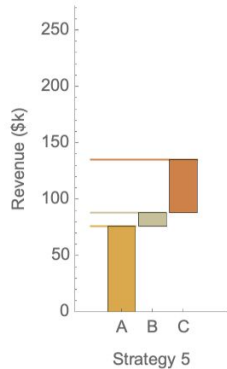
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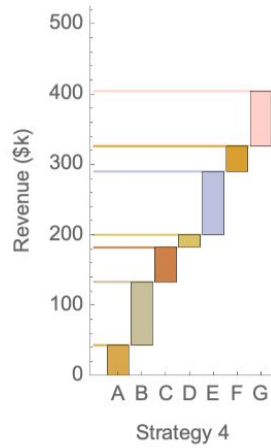
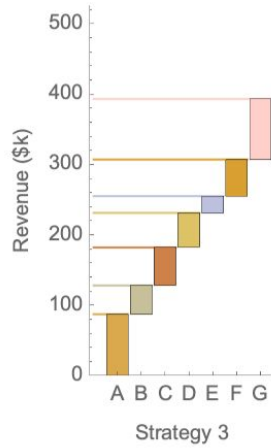
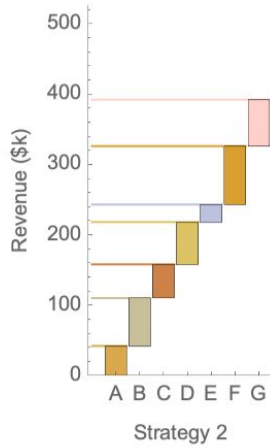
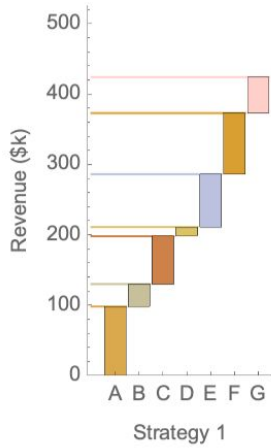
Product Mix Example



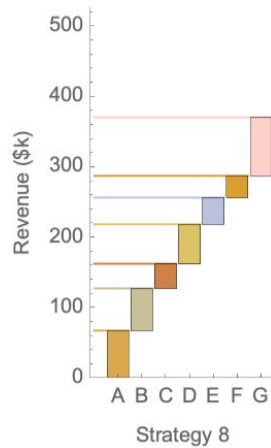
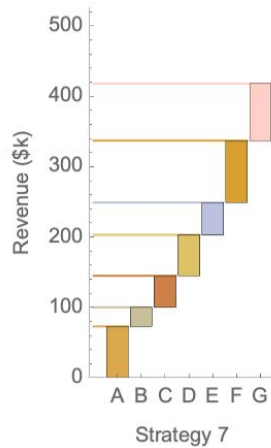
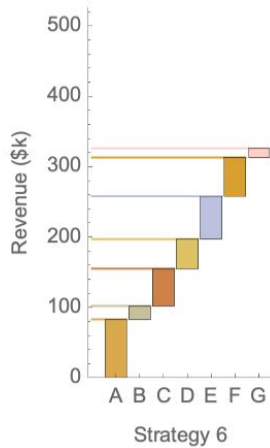
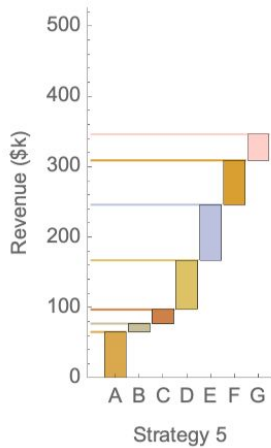
- Product A
- Product B
- Product C

Out[]=

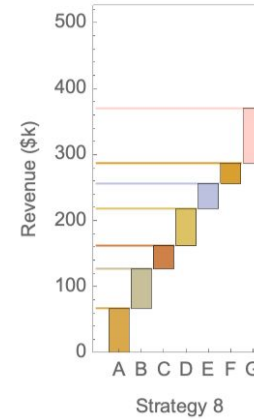
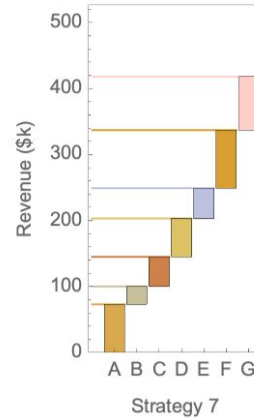
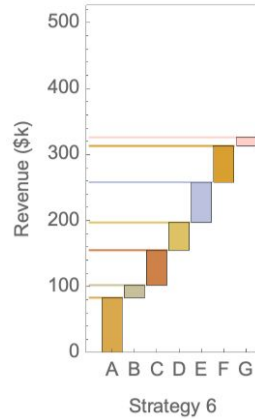
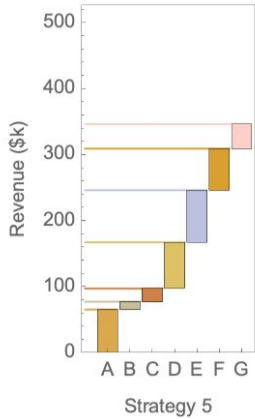
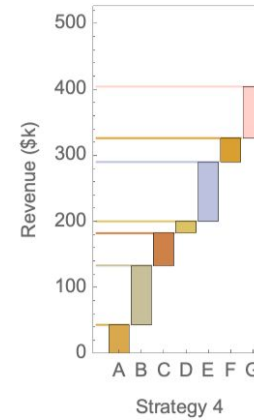
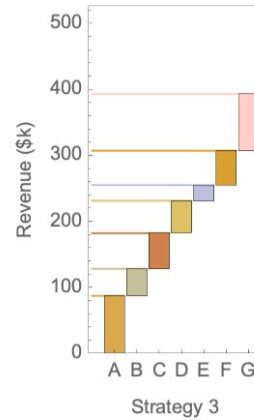
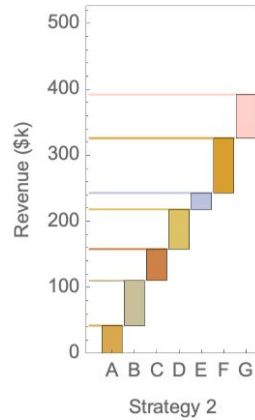
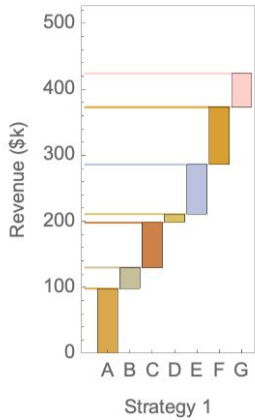


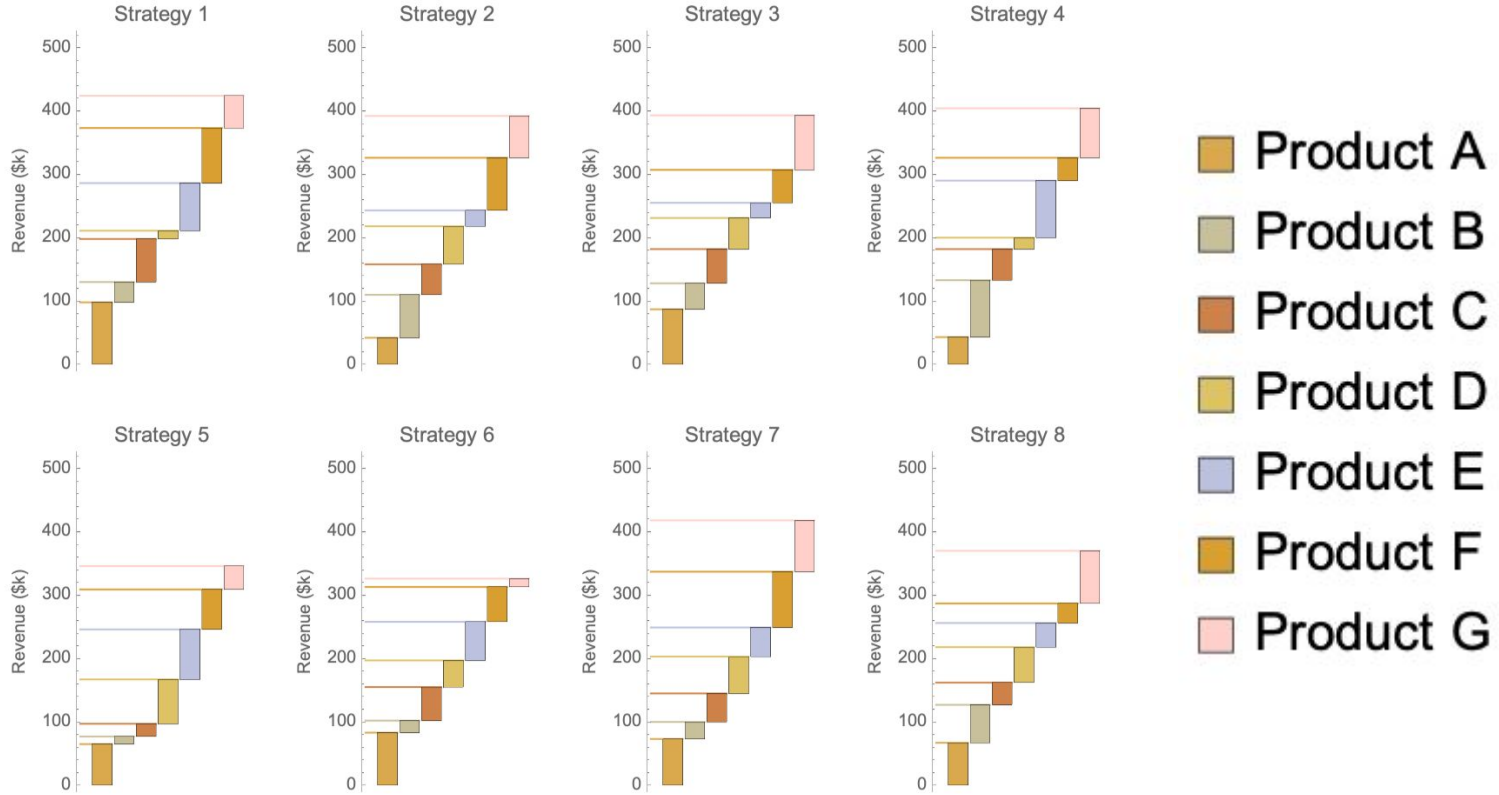


- Product A
- Product B
- Product C
- Product D
- Product E
- Product F
- Product G



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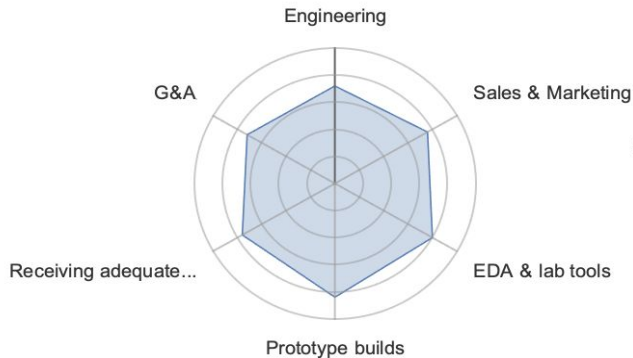


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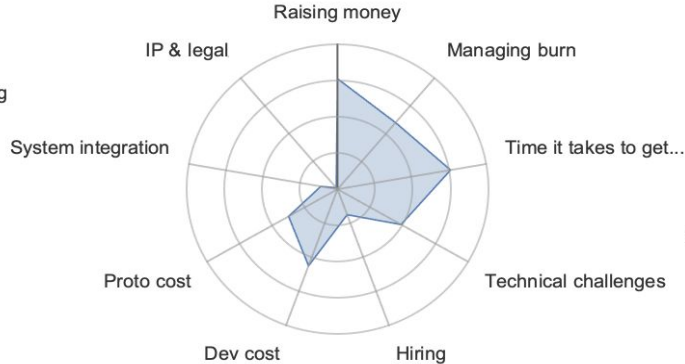
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“It’s difficult to raise money for chip startups with Powerpoint or even simulations”

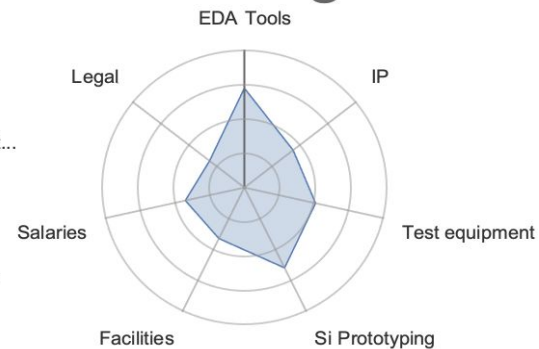
Issues



Expenses

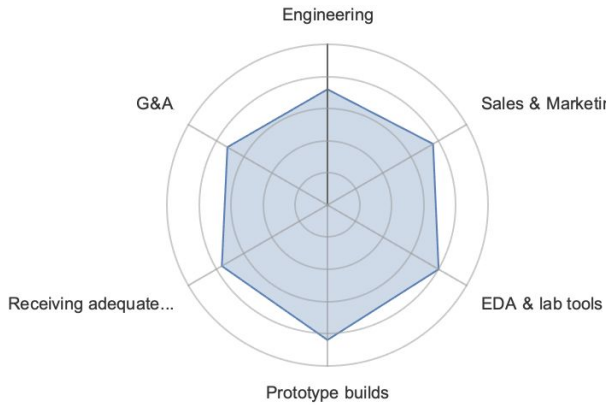


Challenges

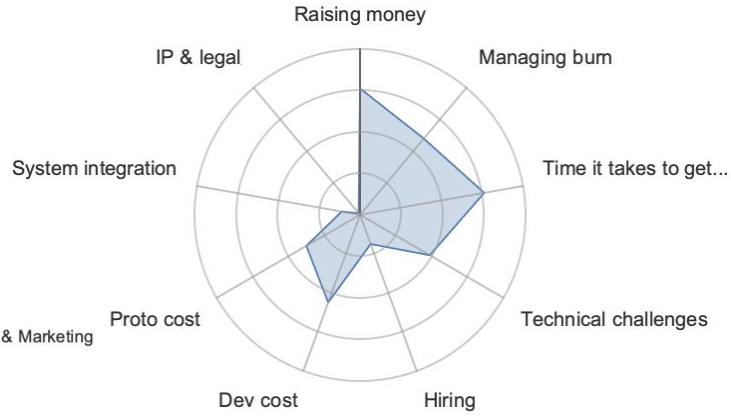


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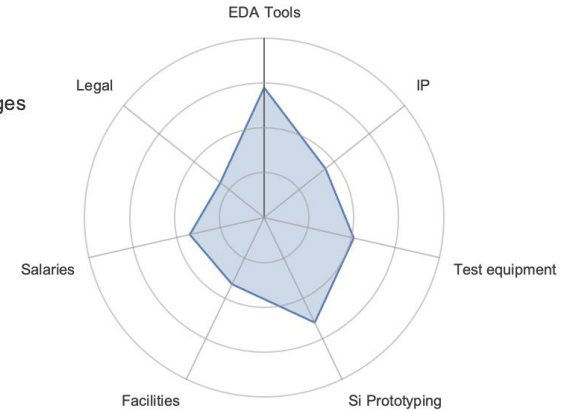
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Rank Issues



Rank Expenses

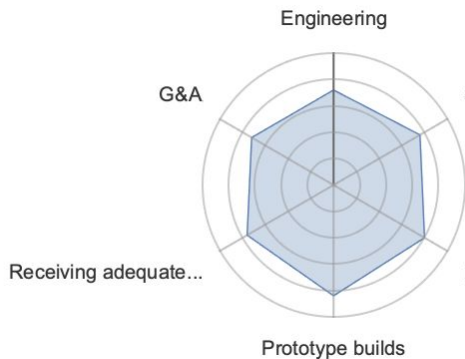


Top Challenges

Source: Silicon Catalyst, 15 startups surveyed in 2014

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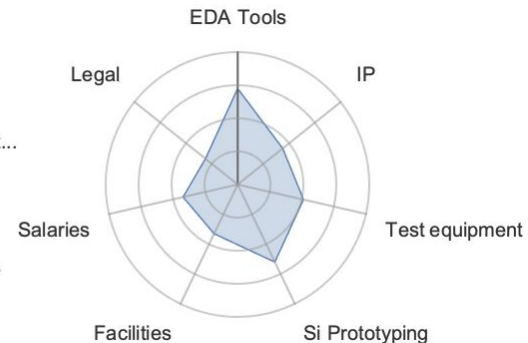
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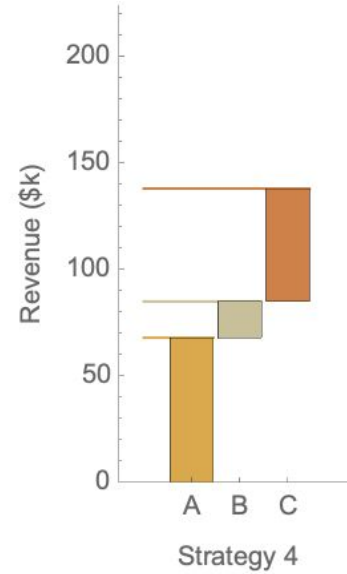
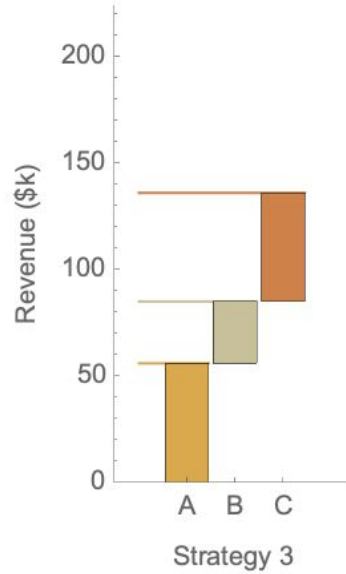
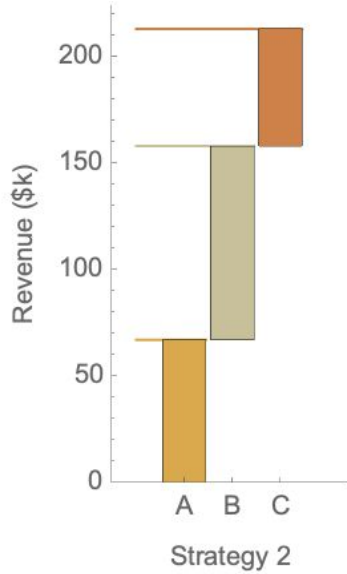
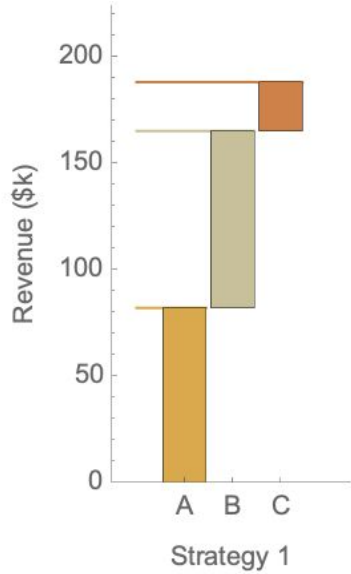
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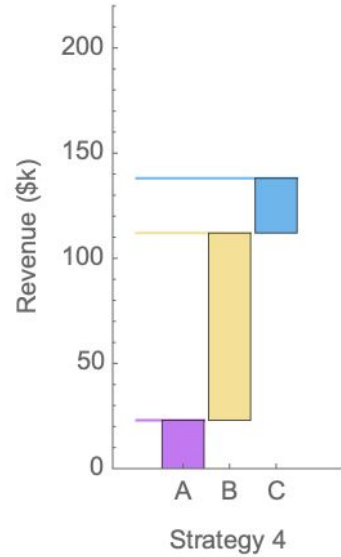
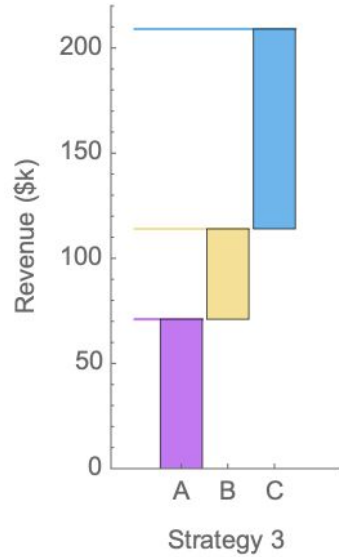
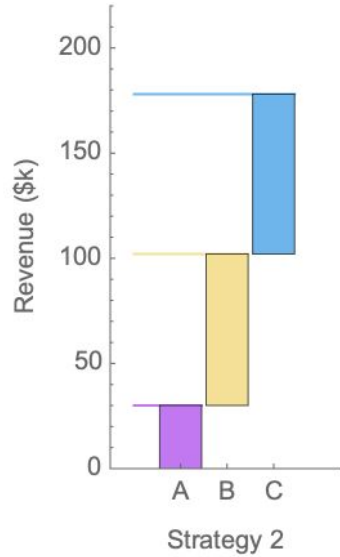
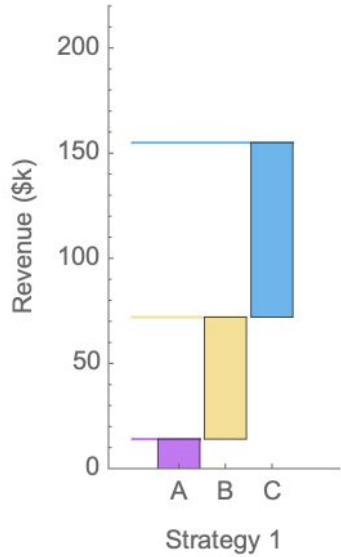
Rank Expenses



Top Challenges



- Product A
- Product B
- Product C



- Product A
- Product B
- Product C