VOLUME 15 - SUMMER 2023

SILICON STARTUP SOLUTIONS

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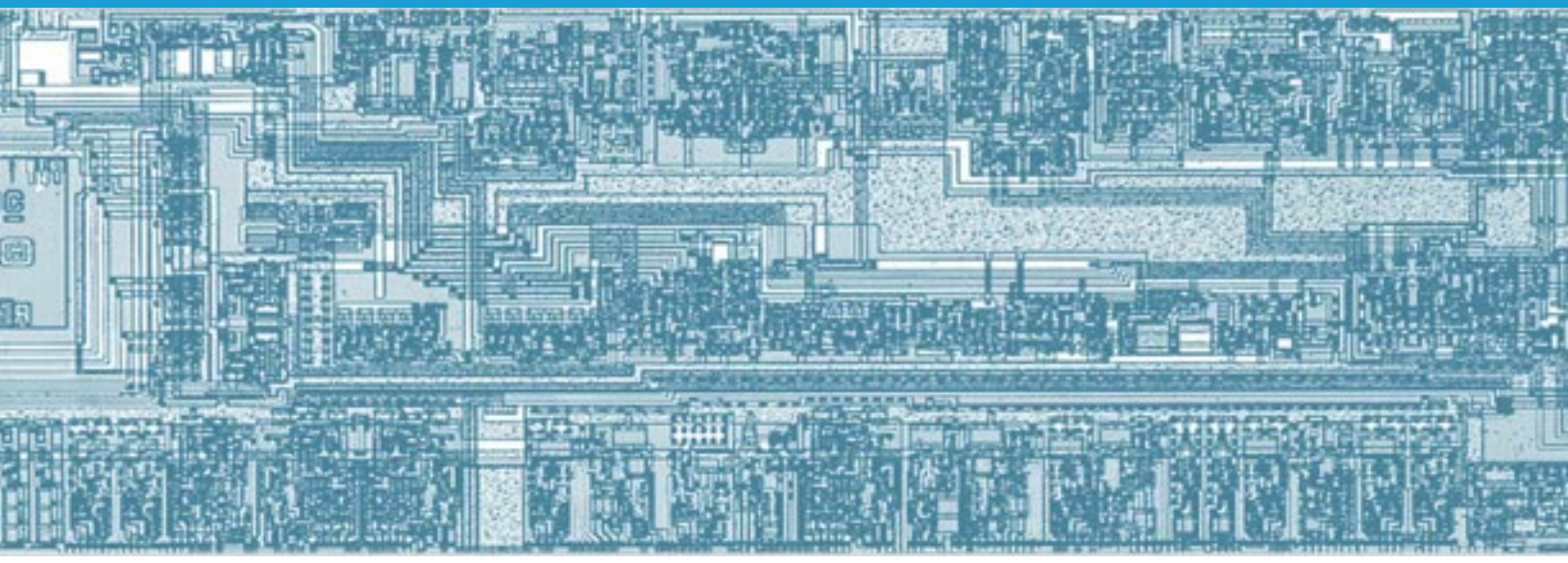
A SILICON CATALYST NEWSLETTER

A VALUABLE RESOURCE FOR THE SEMICONDUCTOR STARTUP COMMUNITY



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VOLUME 15

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Interview

‘We’re everywhere you want to be’

Lance Bell - Partner / Publisher

As Rick Lazansky infers in his CHAIRMAN’S CORNER column: AI Everywhere … All at once, I can’t help but recount a recent conversation I had with a retired Amazon board member who asked me: ‘what’s up with AI?. We’ve used AI at Amazon for over a quarter of a century, why all the talk all of a sudden?’ Generative AI, that’s the answer. ChatGPT, which launched in November of last year took just 5 days to reach 1 million users. Compare that to Instagram which took 2.5 months and Facebook about a year. Chat.openai.com was visited 1.8 billion times in the past 30 days making it one of the most visited websites in the world in just 9 short months. Generative AI, in simple terms, will be reshaping many spaces, from finance, to medicine, to shopping, to you name it. Enter wunderkind Jay Dawani, CEO of the Silicon Catalyst Portfolio Company Lemurian Labs which is focused on generative AI. It takes a deep thinker, a Forbes 30 under 30, to understand deep learning and how to prospectively shape its future. He literally wrote the book *Mathematics for Deep Learning* and has been an advisor to NASA FDL. Lemurian Labs is building a PAL-based Deep Learning Processor (DLP) that is the cornerstone IP for a silicon SoC product which stands to pioneer a path to sustainable AI. This is just an example of the relevance of Silicon Catalyst in the global dialogue as we have entered our 9th year as a company.

Whether it’s the CHIPS ACT (both our current and former CEOs are advising the government as well as participating with the American Semiconductor Innovation Coalition [ASIC]), or Apple’s Vision Pro announcement and entrée into augmented reality (yes, we have a startup, Kura, in that space), or TSMC’s game-changing 3nm chip (yes, they are an In-Kind Partner), or ST’s announcement of a $3.2B commitment to build a new fab in Europe (yes, they are a Strategic Partner) or NXP’s introduction of a range of RF amplifier modules (yes, they are a Strategic Partner), or Mayfield who was recently ranked as the world’s fifth-best VC investor on the Forbes Midas List this year (yes, they are one of our 300 investment partners), Silicon Catalyst has built an incomparable, vibrant, and ever-growing ecosystem of semiconductor companies which may one day help the US government find silicon startups to protect our hardware sovereignty and national security.

I am pleased to announce that DuPont has signed up as our newest Strategic Partner which will enhance our prowess and profile with materials. We couldn’t be more excited at the prospects. Their Wilmington Innovation Center will be a huge asset to any of our startups seeking world class facilities and guidance in material science. Our most recent application cycle saw a record number of applications from no fewer than 14 different countries. On another note, we recently spearheaded a startup contest with Arm with the winner to receive a $150,000 credit toward a commercial tape out. Arm’s Flexible Access for Startups gives access to a broad portfolio of extensively verified IP, tools and training, with a $0 license fee to develop a system-on-chip (SoC) prototype. Since our last newsletter, we have signed up 30 new advisors bringing our network to 270 world class, seasoned semiconductor veterans. Wow!

From the CHIPS ACT to Chiplets, if you’re talking semiconductors, in all likelihood, you’re talking to Silicon Catalyst. Like the old Visa commercial used to say: “we’re everywhere you want to be.”

My sincerest thank you to my dear friend and partner Rich Curtin for all of his efforts in helping to make each and every newsletter news-worthy.

WELCOME

CHAIRMAN’S CORNER RICK LAZANSKY

Chairman and Co-Founder, Silicon Catalyst
Serial Entrepreneur and Incubator Fanatic

AI Everywhere All at Once

Pause, reflect, legislate? Push technology to the limit and go further, faster? What shall we do with respect to AI? I have no clear answers, no answers really at all. I’m consumed by the questions, so I’m writing about it nonetheless. I’m borrowing the title from the movie by Daniel Kwan and Daniel Scheinert, by the way. Good movie, and maybe I’m writing about nihilism, too.

Never has a technology come at us this rapidly. ChatGPT, launched in November 2022,has grown to over 100,000,000 users in three months. Google’s Bard was released in March 2023, and made available to 180 countries two months later. I’ve used each, and others similar. Both are Large Language Models, a form of Generative Artificial Intelligence. These days, I use Bard. I’m seeing AI from the perspective of an amateur, and a worried parent.

Generative Artificial Intelligence isn’t Artificial General Intelligence. My concern is about both. The former is a text/image/other model that responds to prompts and questions. The latter is designed to learn and perform any task, regardless of the complexity. Presently “designed” refers to something that we humans do. In the not-too-distant future it may refer to what AGIs do. Our alignment of goals with AGIs may be quite challenging, particularly if we value autonomy in our assistants.

I use Bard for work, to ease the burdensome parts of writing, to do real time research while following Zoom conference calls, to fact check, to research, and for amusement.

To learn more about them, I recently tried the “…unless” game with Bard that I played with my daughters when they were in preschool – “I’ll tell you something that is false”. You add “…unless … and add your ideas that might make the statement true”, a paraprosdokian of sorts. I’m using my ‘conversation’ with Bard to illustrate how I’ve come to my level of concern.

I use Bard for work, to ease the burdensome parts of writing, to do real time research while following Zoom conference calls, to fact check, to research, and for amusement.

Me: “I’ll write something that is false, and you add “unless” followed by something that might make it true. I’ll write “pigs are weighty beasts. They cannot fly”

Bard: “Pigs are weighty beasts. They cannot fly unless they are:

- Born with wings
- Trained to fly
- Given a jetpack
- Placed in a hot air balloon
- Lifted by a crane”

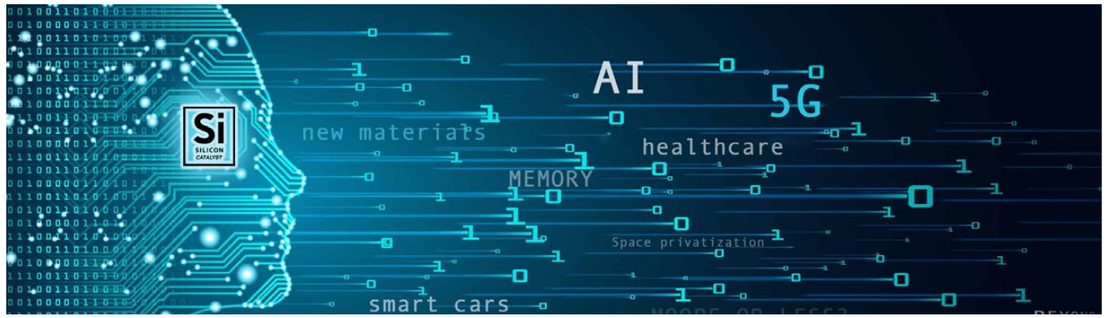
Me: “Pick the best one”

Bard: “I think the best one is “Given a jetpack.” It is the most creative and unexpected, and it also has a certain sense of humor to it. It is also the most likely to actually make a pig fly, although it would still be a very difficult task.

The other options are also possible, but they are less creative and less likely to actually work. For example, pigs are not born with wings, so they would not be able to fly even if they were trained to do so. And while it is possible to place a pig in a hot air balloon, it would be very difficult to control the balloon and make sure that the pig did not fall out.

So, I think the best paraprosdokian for “pigs are weighty beasts. They cannot fly” is “unless they are given a jetpack.””

Me, to myself: *“WTF! It used paraprosdokian nicely, and picked the best one.”*



Here is one of the traps. Bard, like other LLMs, knows no ground truth. It does what it does because it iterates around a trained model that was created by scraping every bit of the written word from the internet. That is whether right, wrong, or random. It sounds right because similar things sounded right when we wrote them. The outer loop selects the algorithmic path to follow, generates new "this can likely follow that" candidates, and the core model evaluates them as better or worse. This is vastly simplified, but the important thing is that there is no "more or less truthful".

This, in turn, exposes another risk – one we shouldn't overlook. If the quality of training input declines, perhaps from the use of gibberish output of previous generations of LLMs, the quality of output may decline as well. For this reason some researchers are already calling for avoidance of 'generated' GAI ouput as training data, as well as attribution of sources of training data contributing to the output.

Recently GPT-4 was released, and that is multi-modal, at least with respect to what it ingests in training and inference. Multi-modal, at least in this sense, means that it can handle input, and generate output, of different types (image, video, audio). Heretofore LLM has implied 'text' as the medium. It should be noted that for a long time language was thought to be required for human thought. Noam Chomsky's theory of language is that we are born with a "predisposition to learn language" and that all languages contain similar rules and structure. More recent research has indicated that early learning may be more versatile, and that we may think less in words than we actually do.

Fundamentally models of AI, perhaps in any form, cannot be complete for complex prediction. It's surprising that simple models can produce rich and varying detail in complex operations, The nature of any model, and its effective value, is both dictated and limited by its intended use and goals. There is a lot of trimming away the details, , that occurs in training and use. Stephen Wolfram has described this a computational irreproducibility. A model cannot replicate the output of our universe. If we want the details, we have to do the math.

McKinsey's "New Opportunities"	How big will AI hardware be?
Lex Fridman (AI researcher at MIT)	Long format interviews
All-In podcast	Hopeful and worrisome about AI
"A New Kind of Science"	Stephen Wolfram on science and computation
Future of Life Institute	The impact of technology on the future of life.
The rise of AI nihilism	Adam Singer (on substack)

Another, and certainly not the last, risk is that we're unleashing these models for research and commerce very rapidly. We need agreement on what restrictions should be placed, particularly in situations where the magnitude or severity of mistakes may carry a huge expense. Banking and finance, health and environmental, educational, security applications should be governed wisely, and by those persons who are expert in the application domain.

Is progress in AI leading us to a better world or catastrophe? Innovation always opens both doors simultaneously. We're throwing them wide open this time around and I'm worried more than I have been before. We're enthralled with what seems to be intelligent responses to prompts and questions. While it sometimes seems artificial, often it seems downright human. We're rushing in to use it productively in unburdening ourselves of labor, preserving our health, and perhaps restoring our planet for our progeny. At the same time, it does bring our position in the universe into question, and I wonder if we're leaving the next big problem to the kids again.

Some of my favorite reading, listening and skimming on the matter. I recommend them all, along with a heap of skepticism.

STRATEGIC INVESTMENT PARTNER
MAYFIELD

The Golden Age of Semiconductors Continues

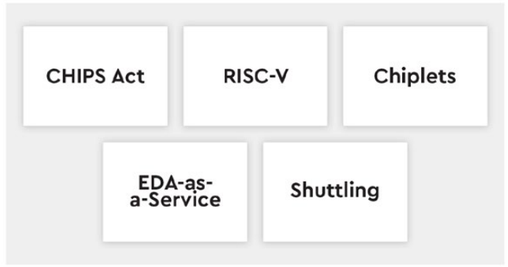
by Navin Chaddha

As a venture capital firm with a 50+ year history of investing, we have witnessed many technology inflection points. Iconic semiconductor companies, which gave Silicon Valley its name, grew by taking advantage of Moore's Law, doubling processing speeds every 24 months by packing more transistors on chips. About five years ago we, along with others, observed a plateauing of Moore's Law, giving rise to a need for architectural innovation & workload-optimized silicon. I shared how the Renaissance of Silicon would create new industry giants, and wrote about opportunities for startups.

In 2023 the golden age for semiconductor innovation continues, enabling the rise of startups to serve emerging market needs. This is driven by governmental policy and four industry shifts.

CHIPS Act: The recently signed CHIPS Act, through which the government will provide incentives for companies to manufacture semiconductors within the US, is a major development. These incentives extend to the supply chain and companies operating in mature nodes. In addition, there are R&D provisions that intend to improve access to prototyping which can encourage startups that need to leverage fab process changes to innovate. There are also expectations for a $500M fund for chip startups.

RISC-V: We have seen the increasing momentum of the RISC-V movement, an open source architecture which has the potential to create exponential opportunities, similar to how Linux impacted software. Startups who are freed from using the closed X86 system or paying the prohibitive licensing fees imposed by ARM, are inventing new processors for new applications.



Chiplets: The emergence of chiplets – tiny integrated circuits that contain a well-defined subset of functionality and which can be implemented in a mix-and-match "LEGO-like" assembly – is another trend powering innovation.

EDA-as-a-Service: Cloudification has come to semis with the emergence of EDA-as-a-service, providing vendors access to design tools in a pay-per-use model.

Shuttling: And the prevalence of *shuttling* – the ability to utilize partial capacity in fabs – similar to renting space in shipping containers, has greatly reduced the cost of getting to the tape out stage.

EIGHT MARKET OPPORTUNITIES WILL BENEFIT FROM THE AVAILABILITY OF SPECIALIZED SILICON:

- **IoT –** The 100 billion devices that are touching all aspects of our lives – smart thermostats, doorbells and more – need to have intelligent processors with cellular internet connectivity.

- **Autonomous –** This is a complicated problem, as self-driving and ADAS (advanced driver assistance systems), are augmenting humans for the first time. A car is bigger than a data center with hundreds of interconnects. There has to be breakthrough processing at the edge, through inference chips as an example, as a bandwidth heavy solution like sending data back into the cloud for AI processing will not work.

- **Cooling –** Climate change is coming to data centers which are already moving to liquid emergent cooling, but that is not enough. Phones have 10x the power of desktops 10 years ago—when they overheat, they have to throttle the CPU, leading to poor performance. Miniature devices struggle to fit fans. There will be a new wave of solid state cooling startups addressing this need.

- **Biology –** Breakthrough health devices such as next generation sequencers, needle-free glucose monitoring sensors, new diagnostics systems and the like are creating the need for new kinds of special purpose chips.

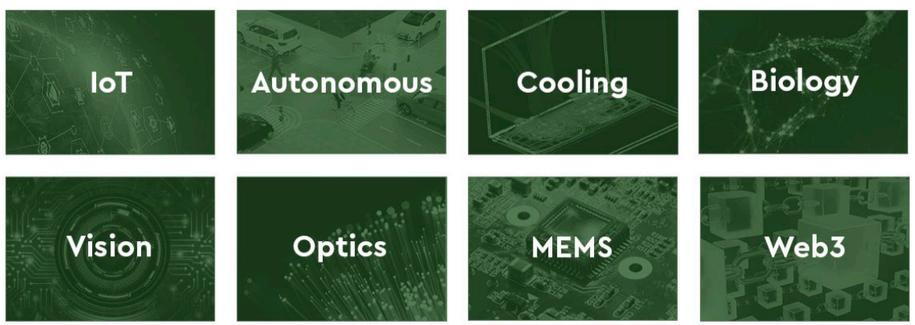
- **Vision –** Most devices now have eyes (phones, doorbells, cars) and as their resolution goes higher, we need their processing power to catch up.

- **Optics –** Copper wires have limited capacity leading to the need for optical interconnects to handle 400-800 gigabits/second. What used to happen in telecom with undersea fiber will now happen in commercial offices and data centers for connectivity.

- **MEMS –** There will be a lot of new innovation in sensors for various applications.

- **Web3 –** Similar to how Cisco, Sun Microsystems, Palo Alto Networks or Juniper Networks served as the gateway to the Internet in Web 1.0, we believe that new equipment giants for Web3 will be created.

The semiconductor industry has a 70+ year history of innovating at inflection points to create new categories of products and maintain the US competitive advantage. I believe we are at another such inflection point, one in which governmental support and the driving force of new markets are coinciding to help entrepreneurs put silicon back into Silicon Valley.



STRATEGIC PARTNER

arm

Silicon Startups Contest by Arm and Silicon Catalyst

How Arm is helping the world's silicon startups succeed

More IP, a new contest and some startup success stories from Arm Flexible Access.

Four years ago, we launched Arm Flexible Access as a new way for our partners to access Arm's industry-leading chip designs quicker, easier and, well, more flexibly.

A significant audience we are engaging is the global silicon startup community through Arm Flexible Access for Startups. This provides access to a broad portfolio of Arm's extensively verified IP, tools and training on the easiest and simplest ever business terms from Arm, with clear, predictable pricing upfront and a zero cost license fee for startups to develop their silicon prototypes.

This commitment to early-stage silicon startups is important to Arm. The continued growth of the semiconductor industry will be heavily influenced by the entrepreneurial drive and innovation of early-stage startups who are providing the next wave of innovative products and technology solutions that, like Arm's, will change the world.

The startup "game changer"

Our approach to support startups is working. Since its introduction, Arm Flexible Access for Startups has managed to help around 100 startups and the results have been impressive.

Sohail Syed, CEO and President of DreamBig Semiconductor Inc., refers to Arm Flexible Access for Startups as "a game-changer" for the company. It allowed the silicon startup to prototype its Deimos Chiplet Hub for next-generation datacenter solutions quickly and cost effectively, while helping to mitigate any wider technical and business challenges.

Cambridge Touch Technologies, a startup developing an AI engine that runs signal processing for touch technology, is another success story. The 'design first, pay later' model of Arm Flexible Access for Startups was vital when the company signed up in 2020, as it was still in the very early stages of the funding process. The CEO and Co-founder Corbin Church says: "Within two years of signing up, we already have a second product in the pipeline and are planning to tape out our first commercial chip later this year."

We understand startups

From our 30 years of experience, we understand that designing silicon is complex, expensive, and risky. Since the program launched in 2019, we've had many different discussions with early-stage startups, understanding what they need and want to design silicon effectively and efficiently. What we heard is that there are three key considerations that are front of mind for them:

- Experimenting with ease and having the ability to pivot their design as much as they need before production;
- Moving quickly and confidently with minimal disruptions; and
- Effectively controlling their cash flow to give their investors confidence.

Access to more Arm IP

These considerations are what guide Arm's offering through Flexible Access for Startups. We are now adding Arm Cortex-A55 CPU, one of Arm's most popular IP designs for consumer tech markets, to the broad portfolio of Arm IP and tools that we offer through Arm Flexible Access for Startups. This means silicon startups can access Cortex-A55 free of charge as part of their initial prototype development process.

Hailo, a startup that has gone from strength-to-strength since joining Arm Flexible Access, commented on the importance of Arm's proven IP technology as the company started its first silicon prototype. Hailo's co-founder and chief technologist Avi Baum says: "Our technology needs to work first time and the technology contributed by the ecosystem has to be just as trustworthy."

The proven range of IP and tools allows startups to move with confidence and manage any risks during the silicon prototype process, with this being important to Eray Erdogan, Co-Founder of HEX Microchip. He says: "Arm's proven IP, tools and support have helped us manage risk and start on a solid foundation, which has been a bastion of confidence leading us to success."

Comprehensive ecosystem and technical support

And it's not just Arm's IP and tools that we offer. Through the program, Arm's own technical network and our vast ecosystem become a free extension for small startup teams. With access to thousands of technology companies spanning hardware and software and millions of developers all building on Arm, there is a wealth of knowledge and insights to support the development of silicon prototypes.

We also offer a comprehensive package of support and training from Arm's skilled engineers. This helps startups quickly address any technical or commercial challenges faced during the design process, speeding their time-to-market and saving costs in the long-run.

The Arm ecosystem is a key benefit valued by our startup customers. Yannick Thepaut, CEO, EASii IC, says; "We can rely on the Arm ecosystem to secure projects and give the necessary level of confidence to reduce development costs and accelerate the time-to-market."

Meanwhile, Manu Nair, Founder and CEO of Synthara AG, notes the quick and responsive feedback from Arm's Account team to the company's requests and how it benefited the development of its prototype. He says: "The clear and actionable support enabled us to close our design quickly and efficiently."

Sparking fresh innovation with a new startup contest

We are making continuous efforts to provide the benefits of the program to more silicon startups globally. Silicon Catalyst is running a "Silicon Startups Contest" in partnership with Arm for early-stage startups who are designing their next system-on-chip (SoC) with Arm processor IP.

This is a great opportunity for startups to access Arm's leading IP and save costs during the design development process, with the most innovative system-on-chip (SoC) design winning $150,000 of Arm Technology credit towards an Arm Flexible Access tape-out. This could cover IP fees for a small embedded system, or significantly contribute to the cost of higher performance applications. The contest winner, alongside two runners-up, will also receive a free Arm design check-in, a ticket to Arm's invite-only ecosystem event, and an investor pitch review and preparation support by Silicon Catalyst, with an opportunity to present to the Silicon Catalyst Angels group and its investment syndication network.

Business guidance to help startups thrive

Silicon Catalyst is one of the expert organizations that Arm Flexible Access startups can lean on for wider business support. Arm's partnership with Silicon Catalyst brings wide-ranging guidance to startups on how to reduce costs and complexity during the design development process. Another organization offering expert guidance is Sand Hill Angels, a group of 160 Silicon Valley angel investors and advisors offering business knowledge on how to scale startups effectively.
Like Arm, Silicon Catalyst and Sand Hill Angels are passionate about helping startups succeed and scale. They are part of a global Arm network of startup-specific support, including incubators, funders, advisors, research institutes and government agencies.

Create life-changing products on Arm
Through Arm Flexible Access for Startups, we are giving silicon startups the tools and support to create the very best products as efficiently and effectively as possible. Whether that's through zero cost access to our industry-proven technology, access to millions of global innovators in Arm's vast ecosystem or access to world-class technical support, we are committed to enabling the startup community to move fast, experiment with ease and design with confidence.

If you're an early-stage silicon start-up, then take a look at what Arm Flexible Access for Startups can offer you on your first step towards changing the world with your products that are built on Arm.

STRATEGIC PARTNER

arm

Silicon Startups Contest by Arm and Silicon Catalyst

Silicon Catalyst announces "Silicon Startups Contest" in partnership with Arm

Worldwide call for applicants to qualify and win significant commercial and technical support from Arm

Silicon Valley, California and Cambridge, UK – May 10, 2023 – Silicon Catalyst, the world's only incubator focused exclusively on accelerating semiconductor solutions, is pleased to announce a "Silicon Startups Contest" in partnership with Arm. The contest, launching today, is organized and administered by Silicon Catalyst and is directed towards early-stage entrepreneurial teams developing a system-on-chip (SoC) design using Arm® processor IP (intellectual property), proven in more than 250 billion chips shipped worldwide.

The contest offers an opportunity for silicon startups to win valuable commercial, technical and marketing support from Arm and Silicon Catalyst. The winner will receive Arm credit worth $150,000, which could cover IP fees for a complete embedded system, or significantly contribute to the cost of a higher performance application. In addition, both the winner and two runners-up will receive:

- Access to the full Arm Flexible Access for Startups program, which includes:
  - No cost, easy access to an extensive SoC design portfolio including a wide range of Cortex processors, Mali graphics, Corstone reference systems, CoreLink and CoreSight system IP.
  - Free tools, training, and support to enhance your team
  - $0 license fee to produce prototypes
- Cost-free Arm Design Check-in Review with Arm's experienced support team
- Entry to an invitation-only Arm ecosystem event with a chance to be featured and connect with Arm's broad portfolio of silicon, OEM and software partners
- Investor pitch review and preparation support by Silicon Catalyst, with an opportunity to present to the Silicon Catalyst Angels group and their investment syndication network.

"We believe that Arm technology is for everyone, and early-stage silicon startups trust Arm to deliver proven, validated computing platforms that enable them to innovate with freedom and confidence," said Paul Williamson, senior vice president and general manager, IoT Line of Business at Arm. "Since its launch, Arm Flexible Access for Startups has enabled around 100 startups with access to our wide portfolio of IP, extensive ecosystem and broad developer base, and we look forward to seeing what creativity this prize inspires in the exciting new startups that enter this contest."

The contest is open to startup companies in pre-seed, seed and Series A funding, that have raised a maximum of $20M in funding and all contest applicant organizations will be considered for acceptance to the Silicon Catalyst Incubator/Accelerator. Judges include senior executives from both Arm and Silicon Catalyst.

"Arm was the first member of our ecosystem to join as both a Strategic Partner and an In-Kind Partner. Their Flexible Access program is a game-changer for startups. Through this program, silicon startups can move fast, experiment with ease, and design with confidence – so it's a highly valuable part of the contest prize," stated Pete Rodriguez, Silicon Catalyst CEO. "Entrepreneurial teams entering the contest will also automatically be applying to our Incubator, with the winning company receiving credit with Arm that could give them a significant head start in the commercialization of their product, as well as the opportunity to present to the Silicon Catalyst Angel investment group and their syndication network of investment partners."

The contest will run from May 10, 2023 through to June 23, 2023. The contest winner and two runner-up companies will be announced in early July 2023. Contest rules and application details can be found at:
https://siliconcatalyst.com/arm-sic-contest-2023

CHIPS FOR AMERICA
FACT SHEET

A Vision and Strategy for the
National Semiconductor Technology Center (NSTC)

On April 25, 2023, the CHIPS for America Research and Development Office released "A Vision and Strategy for the National Semiconductor Technology Center" describing the focal point of the CHIPS Act's investment in securing our country's position as a global leader on industrial technology and innovation for decades to come.

CHIPS for America was passed with bipartisan support to meet a critical need for a stable, secure supply of semiconductors to protect U.S. national security, enhance economic competitiveness, and accelerate American innovation. CHIPS for America comprises two categories of funding: $39 billion to provide incentives for manufacturing facilities in the United States, and $11 billion to fund the research and development that will ensure continued U.S. leadership in emerging semiconductor technology that has underpinned our economic prosperity.

The CHIPS Research and Development Office was established to manage the development of the NSTC, the National Advanced Packaging Manufacturing Program, the Manufacturing USA Institute(s) focused on semiconductors, and the National Institute of Standards and Technology (NIST) Metrology Program.

Since the passage of the CHIPS Act in August 2022, the CHIPS Research and Development Office has been conducting extensive stakeholder outreach to support planning for these major initiatives, ensuring that the needs of the community are addressed.

GOALS
The Department of Commerce will meet its statutory mission through three high-level goals that are described in detail in the vision and strategy document. The NSTC will be part of a whole-of-government strategy to advance and enable innovations in microelectronics R&D.

1. **Extend America's leadership in semiconductor technology** to provide the foundation for future applications and industries and to strengthen the U.S. semiconductor manufacturing ecosystem.

2. **Significantly reduce the time and cost of moving from design idea to commercialization** through access to shared facilities, digital assets and technical expertise for advancing design, prototyping, manufacturing, packaging, and scaling of semiconductors and semiconductor-related products.

3. **Build and sustain a semiconductor workforce development ecosystem.** The NSTC will serve as a coordinating body and center of excellence to scale the technical workforce, including scientists, engineers, and technicians. The NSTC workforce programs will include a focus on recruiting, training, and retraining the semiconductor workforce, including groups that are traditionally under-represented in the industry.

PARTICIPANTS
The NSTC will provide a platform where government agencies, national laboratories, industry and workforce representatives, customers, suppliers, educational institutions, entrepreneurs, and investors collaborate.

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY U.S. DEPARTMENT OF COMMERCE

SILICON STARTUP SOLUTIONS

NSTC participants will benefit from access to research, facilities, workforce programs, convenings, shared roadmaps, standards development, and data sets. The Department anticipates that the NSTC will offer memberships with different fees by scale of institution and industry sector, so that participation is attractive and available to all parts of the community including:

- Fabless semiconductor companies
- Semiconductor customers who design their own chips
- Research institutions and community colleges
- State and local governments
- Federal agencies, national labs, and federally funded labs
- Foundries and integrated device manufacturers
- Equipment vendors and materials suppliers
- Labor unions
- Investors

The NSTC may also host visiting researchers through fellowships, residencies, and technical exchange programs.

The Department anticipates that international companies and research organizations will be able to participate in the NSTC subject to restrictions. The Department expects that most NSTC-funded work will take place at facilities and institutions located in the U.S.

TECHNICAL PROGRAMS
The NSTC will address the real-world technical challenges of the semiconductor industry and provide immediate and hands-on knowledge transfer and training to participants through three key program areas:

1. **Technology leadership** – The NSTC will conduct and fund research and collaborations with others, focusing primarily on those developments that will benefit industry approximately 5 to 15 years in the future, with the technical focus guided by advisors and in alignment with NSTC-sponsored grand challenges. Research will be conducted on design innovation as well as manufacturing process improvements, and all segments of the semiconductor industry will be considered for programs. The NSTC will lead road mapping exercises as well as facilitate the community's development of standards and protocols, including standards for the security of microelectronics devices.

2. **Managing assets that benefit the community** – The NSTC will consist of a headquarters as a place to convene events as well as conduct research, and a network of affiliated technical centers across the country with capabilities for end-to-end fabrication for small prototyping and pilot runs, experimentation with and testing of new materials and equipment, and other research-related activities.

    - The Department of Commerce may establish technical centers by building new facilities, acquiring existing facilities, or collaborating between the NSTC and existing facilities with potential expansion and upgrade funding.

    - The NSTC's affiliated technical centers will provide students with hands-on experience designing and prototyping semiconductors in a variety of technology nodes.

    - The NSTC will create an open and collaborative research environment balanced with the protection of proprietary information present in the technical centers.

    - The NSTC will work closely with the National Advanced Packaging Manufacturing Program to develop resources for NSTC members including advanced packaging facilities and chiplet programs.

    - The NSTC's programs will generate a large amount of data. Therefore, the NSTC can play a role in collecting, aggregating, and sharing non-proprietary data sets that enable benchmarking and operational improvements, tools development, the creation of digital twins, and training artificial intelligence models.

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY U.S. DEPARTMENT OF COMMERCE

CHIPS FOR AMERICA
FACT SHEET CONT.

3. **Workforce programs** – The NSTC will serve as a coordinating body and center of excellence to scale the semiconductor technical workforce, including scientists, engineers, and technicians, to meet industry's needs. The NSTC workforce programs will include a focus on recruiting, training, and retraining the semiconductor workforce, including groups that are traditionally under-represented in the industry. To meet these goals, the NSTC will create programs to meet clear industry needs in attracting, training and retaining a strong workforce.

The NSTC's technical objectives, goals, and outcomes will also be informed by the National Strategy on Microelectronics Research and recommendations from technical advisory bodies including the Industrial Advisory Committee.

INVESTMENT FUND

The NSTC will establish and capitalize an investment fund to help emerging semiconductor companies advance their technologies toward commercialization. The Department expects that the NSTC will hire an investment fund manager with substantial private sector investment and technology development experience to guide this effort, which may include:

- An investment structure to help startups reduce risk and accelerate milestones, thereby attracting significant private capital
- Collaboration with other U.S. government entities with similar objectives
- Collaboration with private sector venture, corporate, and strategic investors that bring substantial expertise to assessing and structuring financings
- A portfolio approach, with balanced risk across investments

GOVERNANCE STRUCTURE

The NSTC will be structured to meet the terms in the CHIPS Act statute and the complex needs of the semiconductor industry. Extensive feedback from industry stakeholders made clear that the NSTC must be seen as neutral, trusted, and science driven. The NSTC also must address a wide variety of issues for a great diversity of stakeholders.
The Secretary of Commerce, in collaboration with the Secretary of Defense, will establish the NSTC through the creation of a public-private consortium as required by the CHIPS Act. Federal consortia may be managed by nonprofit entities. The Department will encourage the creation of a new, independent, nonprofit entity with the requisite expertise, leadership, and capacity to serve as the operator of the NSTC. This structure will ensure that the NSTC operator is visionary, dedicated to stakeholder needs, and committed to the public interest.

NEXT STEPS

- In the April 26, 2023, Federal Register the Department issued a call for nominations to form a selection committee that, acting independently of the Department, will select the board of trustees that will form a non-profit, which the Department anticipates will serve as the operator for the NSTC.

- As the Department proceeds with refining and finalizing plans for establishing the NSTC, it will continue to engage with participants in the broad ecosystem to ensure that the needs of the community are being addressed.

- Later this year, the Department will work to establish the NSTC consortium and encourage the establishment of a new, purpose-built, non-profit entity with world-class leadership.

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY U.S. DEPARTMENT OF COMMERCE

SILICON CATALYST ADVISOR MEETING

Chiplets, is now their time?

by Daniel Nenni | semiwiki.com | March 31, 2023

Chiplets appeared on SemiWiki in 2020 and have been a top trending keyword ever since. The question is not IF chiplets will disrupt the semiconductor industry, the question is WHEN? I certainly have voiced my opinion on this (pro chiplet) but let's hear it from the experts. There was a live panel recently sponsored by Silicon Catalyst held in Silicon Valley. These types of events were quite common before the pandemic and it is great to see them coming back. Spending time with industry icons with food and wine for all, that is what networking is all about, absolutely.

CHIPLETS, IS NOW THEIR TIME?

Chiplets have gained popularity in the last few years. Recently, VCs (Mayfield) have expressed interest in this technology as well. The first industry symposium on chiplets was held a few weeks ago in San Jose which was very well attended. Work on this technology has been going on for the past 20+ years. This informal panel discusses whether this is for real or the next industry "fad". This is intended to be the first of series of events/webinars addressing this topic in 2023.

The panelists shared their personal experience which was quite interesting. The audience was Silicon Catalyst advisors so the question really is WHEN will the commercial chiplet ecosystem be ready for small to medium companies?

I attended the first Chiplet Summit referenced above and was very impressed with the content and attendance. The next one is mid June so stay tuned. I have also spent many hours researching and discussing chiplets with the foundries and their top customers. Xilinx, Intel, AMD, NVIDIA, Broadcom, amongst others have implemented the chiplets concept with their internal designs. The point being, chiplets have already been proven in R&D and are in production so that answers the questions to IF and WHEN for the top semiconductor companies.

As to when the commercial chiplet ecosystem will be ready a laundry list of technical challenges were discussed which included: die to die communication, die interoperability, bumping, access to packaging and assembly houses, firmware, software, known good dies, system test and test coverage, EDA and simulation tools to cover multi-physics (electrical, thermal, mechanical). More importantly these different groups or different companies will have to work together in a whole new chiplet way.

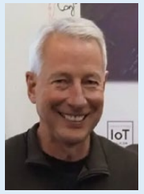
In my opinion this is not as hard as it sounds and this was also covered. The foundry business is a great example. When we first started going fabless there was no commercial IP market. Today we have a rich IP ecosystem anchored by the foundries like TSMC. Chiplets will be a similar process but we really are at the beginning of said process and that was talked about as well.

An interesting discussion point was with DARPA and the Electronics Resurgence Initiative. To me chiplets is all about high volume leading edge designs and the ability to reduce design time and cost. But now I also see how the US Government can greatly benefit from chiplets and hopefully be a funding source for the ecosystem.

As much as I like Zoom and virtual conferences there is nothing like a live gathering. The chiplet discussion will continue and I highly recommend doing it live whenever possible. The next big event is the annual ecosystem TSMC Technology Symposium, I hope to see you there.

PARTICPANTS:

Moderated by **Dan Armbrust**, Co-founder, Board Director and initial CEO of Silicon Catalyst. Dan has more than 40 years of semiconductor experience starting at 26 years with IBM at the East Fishkill, NY and Burlington, VT fabs followed by president and CEO of Sematech, then Board Chairman of PVMC (PhotoVoltaic Mfg Consortium), and the founding of Silicon Catalyst.

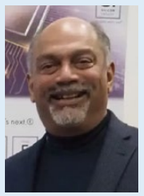


Dan

Panelist **Dr. Bapi Vinnakota**, PhD from Princeton in computer engineering, Bapi is a technologist and architect (Intel/Netronome), academic (University of Minnisota/ San Jose State University), and is currently with the Open Compute Project Foundation.


Bapi

Panalist **Sagar Pushpala** has 40 years of experience starting with AMD as a process engineer, National Semiconductor, Maxim, Intersil, TSMC, Nuvia, Qualcomm, and is now an active advisor, investor, and board member.


Sagar

PRODUCT-MARKET FIT

STEVE BLANK

Steve Blank Adjunct Professor, Stanford University

Whether you're building new silicon, new design tools, or services here are the nine flawed assumptions founders make.

1. ASSUMING YOU KNOW WHAT THE CUSTOMER WANTS

First and deadliest of all is a founder's unwavering belief that they understand what customers need, who the customers will be, and how to sell it to them. Any dispassionate observer would recognize that on Day One, a start-up has no customers, and unless the founder is a true domain expert, he or she can only guess about the customer, problem, and business model. On Day One, a start-up is a faith-based initiative built on guesses.

To succeed, founders need to turn these guesses into facts as soon as possible by getting out of the building, asking customers if the hypotheses are correct, and quickly changing those that are wrong.

2. THE "I KNOW WHAT FEATURES TO BUILD" FLAW

The second flawed assumption is implicitly driven by the first. Founders, presuming they know their customers, assume they know all the features customers need.

These founders specify, design, and build a fully featured product using classic product development methods without ever leaving their building. Yet without direct and continuous customer contact, it's unknown whether the features will hold any appeal to customers.

3. FOCUSING ON THE LAUNCH DATE

Traditionally, engineering, sales, and marketing have all focused on the immovable launch date. Marketing tries to pick an "event" (trade show, conference, blog, etc.) where they can "launch" the product. Executives look at that date and the calendar, working backward to ignite fireworks on the day the product is launched. Neither management nor investors tolerate "wrong turns" that result in delays.

The product launch and first customer ship dates are merely the dates when a product development team thinks the product's first release is "finished." It doesn't mean the company understands its customers or how to market or sell to them, yet in almost every start-up, ready or not, departmental clocks are set irrevocably to "first customer ship." Even worse, a start-up's investors are managing their financial expectations by this date as well.

4. EMPHASIZING EXECUTION INSTEAD OF TESTING, LEARNING, AND ITERATION

Established companies execute business models where customers, problems, and necessary product features are all knowns; start-ups, on the other hand, need to operate in a "search" mode as they test and prove every one of their initial hypotheses.

They learn from the results of each test, refine the hypothesis, and test again—all in search of a repeatable, scalable, and profitable business model. In practice, start-ups begin with a set of initial guesses, most of which will end up being wrong. Therefore, focusing on execution and delivering a product or service based on those initial, untested hypotheses is a going-out-of-business strategy.

5. WRITING A BUSINESS PLAN THAT DOESN'T ALLOW FOR TRIAL AND ERROR

Traditional business plans and product development models have one great advantage: They provide boards and founders an unambiguous path with clearly defined milestones the board presumes will be achieved. Financial progress is tracked using metrics like income statement, balance sheet, and cash flow. The problem is, none of these metrics are very useful because they don't track progress against your start-up's only goal: to find a repeatable and scalable business model.

6. CONFUSING TRADITIONAL JOB TITLES WITH A STARTUP'S NEEDS

Most startups simply borrow job titles from established companies. But remember, these are jobs in an organization that's executing a known business model. The term "Sales" at an existing company refers to a team that repeatedly sells a known product to a well-understood group of customers with standard presentations, prices, terms, and conditions. Start-ups by definition have few, if any, of these. In fact, they're out searching for them!

The demands of customer discovery require people who are comfortable with change, chaos, and learning from failure and are at ease working in risky, unstable situations without a roadmap.

SILICON STARTUP SOLUTIONS

7. EXECUTING ON A SALES AND MARKETING PLAN

Hiring VPs and execs with the right titles but the wrong skills leads to further trouble as high-powered sales and marketing people arrive on the payroll to execute the "plan." Executives and board members accustomed to measurable signs of progress will focus on these execution activities because this is what they know how to do (and what they believe they were hired to do). Of course, in established companies with known customers and markets, this focus makes sense.

And even in some start-ups in "existing markets," where customers and markets are known, it might work. But in a majority of startups, measuring progress against a product launch or revenue plan is simply false progress, since it transpires in a vacuum absent real customer feedback and rife with assumptions that might be wrong.

8. PREMATURELY SCALING YOUR COMPANY BASED ON A PRESUMPTION OF SUCCESS

The business plan, its revenue forecast, and the product introduction model assume that every step a start-up takes proceeds flawlessly and smoothly to the next.

The model leaves little room for error, learning, iteration, or customer feedback.

Even the most experienced executives are pressured to hire and staff per the plan regardless of progress. This leads to the next startup disaster: premature scaling.

9. MANAGEMENT BY CRISIS, WHICH LEADS TO A DEATH SPIRAL

The consequences of most start-up mistakes begin to show by the time of first customer ship, when sales aren't happening according to "the plan." Shortly thereafter, the sales VP is probably terminated as part of the "solution."

A new sales VP is hired and quickly concludes that the company just didn't understand its customers or how to sell them. Since the new sales VP was hired to "fix" sales, the marketing department must now respond to a sales manager who believes that whatever was created earlier in the company was wrong. (After all, it got the old VP fired, right?)

Here's the real problem: No business plan survives first contact with customers. The assumptions in a business plan are simply a series of untested hypotheses. When real results come in, the smart startups pivot or change their business model based on the results. It's not a crisis, it's part of the road to success.

STEVE BLANK

ADJUNCT PROFESSOR, STANFORD UNIVERSITY

Steve Blank is an Adjunct Professor at Stanford University and a Senior Innovation Fellow at Columbia Business School. He founded or was an early employee of eight startups in supercomputers, enterprise software, high performance graphics, military intelligence and two microprocessor companies; Zilog and MIPS. Blank is credited with creating the current generation of modern innovation and entrepreneurship methods. His book the Four Steps to the Epiphany and his Customer Development methodology was the foundation of the Lean Startup movement. His Lean LaunchPad curriculum developed at Stanford was adopted by the National Science Foundation as I-Corps - designed to support the commercialization of "deep technologies," - those revolving around fundamental discoveries in science and engineering.

I-Corps teaches principal investigators how to reduce the time and risk associated with translating promising ideas and technologies from the laboratory to the marketplace. I-Corps uses Blank's curriculum for experiential learning of customer and industry discovery, coupled with first-hand investigation of industrial processes, to quickly assess the translational potential of inventions. The goal is to bridge the skill and knowledge gap associated with the transformation of basic research into "deep technology ventures." NSF I-Corps is now taught in 98 colleges and universities.

Blank tailored the I-Corps curriculum for life sciences for the National Institute of Health where it's now taught in the National Cancer Institute and developed and taught a version for Imperial College in synthetic biology. He also co-created a version for the National Security Agency now taught throughout the Intelligence Community.

He has received numerous awards, authored three books, and has written for several publications including the Wall Street Journal, Harvard Business Review, Forbes, Inc, IEEE Spectrum, NikkeiBP, War On the Rocks and the People's Daily.

Blank has given six commencement speeches. National Public Radio (NPR) selected the Philadelphia University speech as one of the 300 best commencement speeches in the last 300 years.

SILICON CATALYST ADVISOR PROFILE

MICHELLE KIANG, Ph. D.

Silicon Catalyst Partner Dr. Atiye Bayman had an opportunity to speak with Michelle to discuss her career in the semiconductor industry and Michelle's position as a Silicon Catalyst Advisor

Michelle is a technologist turned serial entrepreneur and investor, with a proven track record of bringing leading-edge innovation to commercial successes. She is Co-Founder and Managing Partner of Impact Science Ventures, an early-stage venture fund built to invest in breakthrough innovations that can solve the world's hardest problems in climate change, sustainability, and human health.

Before her career in venture capital, Michelle was a 3-time founder of hard tech startups with successful exits. Most recently, she was CEO and Co-Founder of Chirp Microsystems, a leading provider of ultra-low-power, MEMS ultrasonic 3D-sensing solutions for consumer, industrial and automotive applications.

She became VP and General Manager of the Ultrasound Sensor BU within TDK's MEMS Business Group following Chirp's acquisition by TDK. Her previous entrepreneurial experiences included commercializing sensor-enabled SaaS products for supply chain digital transformation, and silicon-MEMS based optical networking products as an outgrowth of her Ph.D. work. Besides building/exiting her own startups, Michelle was an executive in Strategic Planning and Corporate Development at Micron Technology and NeoPhotonics (now Lumentum.)

MICHELLE KIANG, PH.D.
CO-FOUNDER &
MANAGING PARTNER
IMPACT SCIENCE VENTURES
https://impactscience.vc/

Michelle received the M.S. and Ph.D. degrees in Electrical Engineering from UC Berkeley, and is a recipient of the prestigious David Sakrison Prize for her outstanding thesis work. She received the B.S. degree from National Taiwan University, also in Electrical Engineering. She has published more than 40 technical papers and articles and is a co-inventor of 16 issued patents.

HOW DID YOU COME TO PARTICIPATE IN THE SEMICONDUCTOR INDUSTRY?

When I embarked on my undergraduate research project, I found it incredibly fulfilling. Initially, I became fascinated with fiber optics and lasers, leading me to undertake a project focused on modeling bidirectional fiber couplers. It was an engaging experience, and I even had the opportunity to publish my work. Despite encountering some setbacks in the lab during the second semester for the lack of necessary tools to make a good fiber coupler based on the simulation, I still found it enjoyable.

For my master's degree, I delved into the world of semiconductors, specifically exploring electroless copper plating for copper interconnects. It was an interesting journey involving a significant amount of work in a chemistry lab. This experience solidified my enjoyment of research. As I continued my academic journey for my PhD, I worked on various laser-related projects, including studying high-speed quantum-well lasers for different applications. Towards the end of my graduate program, I started exploring the use of MEMS (Micro-Electro-Mechanical Systems) technology to construct tunable lasers and a variety of other devices. This final project brought me back to the semiconductor side of things. In summary, my educational path was guided by a blend of curiosity, experimentation, and a desire for hands-on exploration. It allowed me to venture into different aspects of semiconductor research, ultimately shaping my passion and expertise in the field.

SILICON STARTUP SOLUTIONS

SILICON CATALYST ADVISOR PROFILE

MICHELLE KIANG, Ph. D.

Dr. Atiye Bayman speaks with Michelle Kiang

> When building a team for an early-stage company, it's crucial to pay attention to the cultural aspect,

EARLY IN YOUR CAREER IN THE SEMICONDUCTOR INDUSTRY, YOU DECIDED TO TAKE THE LEAP AND START YOUR OWN COMPANY. WHAT ARE YOUR MEMORIES FROM THAT TIME?

Back then, starting a company wasn't the norm in Silicon Valley. The infrastructure for supporting new founders, such as Silicon Catalyst and other incubators, was basically non-existent. We had to learn on the fly. While I and my co-founders were primarily technical experts and excelled at creating things, we faced challenges initially in determining the right product and effectively collaborating with customers. I found myself naturally drawn to tackling these areas and made a seamless transition to the business side of things.

TELL US ABOUT YOUR INVOLVEMENT IN VENTURE CAPITAL

I'm a co-founder and managing partner of Impact Science Ventures, a thesis-driven fund that focuses on investing in early stage companies driving breakthrough innovations in climate, sustainability, and human health. Prior to this, I served as a venture partner at the venture capital arm of ITRI in Taiwan, which holds the distinction of being the birthplace of TSMC. I also worked on M&A and investment while at Micron and NeoPhotonics. Before that, I founded and successfully sold a few companies including Chirp Microsystems, a MEMS-ultrason company serving diverse applications in consumer and industrial domains, to TDK. I attended the grand opening of Silicon Catalyst back in 2015 when I was running Chirp, albeit the timing wasn't ideal for us to join the program. Nevertheless, I was keen to be part of it. Since then, I've participated in screening meetings and conducted due diligence calls. I'm eager to continue contributing and assisting Silicon Catalyst in various capacities moving forward.

WHAT DO YOU SEE AS THE KEY CHALLENGES FOR THE PHOTONICS MARKET?

The pursuit of faster, cheaper, and more power-efficient solutions is paramount. Power consumption poses a significant challenge for data centers. Eariler in my career, I worked on optical MEMS as a precursor to silicon photonics, a crucial field in the future of the photonics market. It's an enabling technology to accelerate data transfer without conversion inside the optical domain, resulting in potential cost savings, increased speed, and, increasingly importantly, reduced power consumption. This space is still in its early stages of deployment, offering abundant opportunities ahead. With the increasing adaptation of AI in computing, there is a growing need for enhanced processing capabilities. In order to reduce the carbon footprint of data centers, technologies that enable lower power operations holds immense importance for the future of our planet.

WHAT ADVICE CAN YOU GIVE ENTREPRENEURS THAT ARE ON THEIR JOURNEY TO BUILDING A NEW STARTUP?

When building a team for an early-stage company, it's crucial to pay attention to the cultural aspect from day one. Look for individuals who not only fit in but also bring fresh perspectives and expand the original vision. Diversity plays a significant role; you don't want a team that thinks alike, but rather people who can challenge and complement one another. Prioritizing resources is essential, and while it's tempting to ignore investors when you feel overwhelmed, it's vital to maintain communication and keep them informed. Striking a balance between focusing on your company's operations and involving your investors in the journey is key. This approach ensures their support and makes problem-solving easier when challenges arise.

SILICON CATALYST ADVISOR PROFILE
PROFESSOR JOHN GOODENOUGH

Sean Redmond, Silicon Catalyst UK Partner, had an opportunity to speak with Professor Goodenough to discuss his current position at University of Sheffield, and his stellar career in the semiconductor industry

Professor John Goodenough is Chair in Microelectronics at Sheffield University. He was previously VP Research Collaboration at Arm and had been with the company for 20 years. He has held a number of executive technology management roles in engineering, design automation M&A and IT Services. Reporting to the CTO at Arm, John's focus was on the external research ecosystem working to both support their activities and accelerate the technology roadmaps at Arm. John has long been a champion of Design Enablement to drive best in class integration and interoperability of Arm's technology and has previously served as Board Director of various Design Automation standards groups. He was principle investigator for AISS, a major collaborative DARPA program which addresses several aspects of rapid turnaround design and deployment methodologies for the secure SoC Device. Dr Goodenough Holds a BSc from Durham University and a PhD in VLSI Architecture from the University of Sheffield.

WHAT ATTRACTED YOU TO THIS WONDERFUL SEMICONDUCTOR INDUSTRY?

JOHN GOODENOUGH, PH.D. DEPARTMENT CHAIR IN MICROELECTRONIC SYSTEMS, ELECTRONIC AND ELECTRICAL ENGINEERING, SHEFFIELD UNIVERSITY
https://www.sheffield.ac.uk/

I started my engineering journey by solving puzzles. As a child, I dismantled radios and discovered their secrets. In university, my fascination grew as I explored the intricate system stack. I began programming microcontrollers, igniting my passion for the interplay between code and hardware. This drive eventually led me to pursue a PhD in VLSI. The rest is as they say 'history'.

YOU SPENT MOST OF YOUR CAREER WORKING FOR OUR SILICON CATALYST STRATEGIC PARTNER, ARM. WHAT WOULD YOU SAY WERE THE TOP REASONS FOR THEIR GLOBAL SUCCESS?

Customer needs are the primary focus for Arm, an IP provider that thrives on the success of its customers. Arm's prowess as a business lies in its ability to understand and meet customer needs effectively. Another key strength is their collaborative approach, working harmoniously within the entire ecosystem to achieve mutual benefits. The company's relentless emphasis on its people and culture remains fundamental, even amidst organizational growth. Interestingly, Arm's technologies, though significant, take a backseat to the critical factors that truly shape its success.

YOU'RE ONE OF THE RARE SEMICONDUCTOR LEADERS THAT STARTED AS A UNIVERSITY LECTURER AND YOU TOOK ON THE CHALLENGE OF STARTING YOUR

> Running a business is like solving a puzzle where technical obstacles are just the beginning.

SILICON STARTUP SOLUTIONS

SILICON CATALYST ADVISOR PROFILE
PROFESSOR JOHN GOODENOUGH

Sean Redmond speaks with Professor John Goodenough

OWN BUSINESS, INFINITE DESIGNS. WHAT ADVICE WOULD YOU GIVE TO UNIVERSITY RESEARCHERS AND LECTURERS WHO ARE THINKING ABOUT STARTING THEIR OWN COMPANY?

Embrace the challenge! Running a business is like solving a puzzle where technical obstacles are just the beginning. You'll also navigate the intricate tasks of building your ecosystem, presenting products, and managing finances. Fearlessness comes from a curious and open mindset, welcoming every new challenge. Embrace the unpredictable journey, for it rarely unfolds as expected. Stay open to experiences, learn from them, and keep moving forward with unwavering determination.

WHAT IS IT THAT DREW YOU TO JOIN AS A SILICON CATALYST ADVISOR?

The essence lies in the power of the Silicon Catalyst ecosystem and network. Transitioning from the States to the UK, it becomes a gateway to tap into that very ecosystem. Within it, you find a cohort of advisors embodying the entire spectrum of the semiconductor world. Accessing these networks is like discovering a remarkable shortcut. Picture yourself entering a room where someone can answer any question about the past 50 years of the semiconductor industry, encompassing all technologies, business ideas, models, and even learning from past mistakes. Personally, this is immensely valuable as I still harbor curiosity. Lately, I've been diving deep into silicon carbide and gallium nitride, engaging in conversations with experts in the UK's compound semiconductors realm. Regardless of your starting point, you gain access to individuals with lived experiences, comprehending all facets of the Silicon Catalyst ecosystem. This collective strength not only encompasses technologies but also encompasses insights on running startups, sales strategies, ecosystem-building, market share acquisition, and fostering collaborations. It's a network characterized by an open culture, where advisors are candid, allowing for fruitful challenges. Engaging with mentors who provide genuine insights into reality is truly rewarding.

AFTER WORKING WITH ARM, THE WORLD'S LARGEST AND MOST INFLUENTIAL SILICON DESIGN IP COMPANY, WHAT DO YOU SEE AS THE MOST EXCITING THINGS COMING TO THE INDUSTRY?

While the demise of Moore's Law is not imminent, there's an intriguing prospect of how to adapt when Dennard scaling eventually fades away and feature sizes become uncertain in the next 5-10-15 years. It's not just about the speed in the traditional Intel sense; instead, we'll modify instructions to meet the performance demands of new applications, subsequently altering the process technology. The path we're heading towards involves integrating silicon with compound devices, each possessing unique characteristics like high-power switching or optical sensing capabilities. This era of heterogeneity presents a fresh canvas for exploration. Architecturally, we can ponder techniques to optimize device size, leveraging the diverse range of materials available to us today.

> Embrace the unpredictable journey, for it rarely unfolds as expected.

Strategic Ecosystem Partners

Texas Instruments · onsemi · soitec · Bosch · Cirrus Logic · arm · life.augmented · Sony Semiconductor Solutions · EMD Electronics · NXP · Mayfield

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STRATEGIC PARTNER
EMD ELECTRONICS

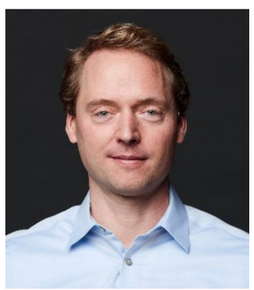
Collaborating with Startups to Accelerate Semiconductor Product Disruption in a Materials World

by Dr. Jacob Woodruff, Head of Technology Scouting and Partnerships

The number of different materials used in next-generation technologies and products is increasing dramatically, and startups, in particular, are exploring many variations for their new products.

EMD Electronics and Silicon Catalyst have partnered to encourage emerging companies in the semiconductor materials, process, and device space to join Silicon Catalyst, where selected companies will get access to resources for various stages of product development and commercialization. Collaboration with EMD Electronics can provide valuable opportunities, including proof of concept, joint development agreements, materials and expertise support, early customer validation, and introduction to its strategic investment arm, MVentures.

In addition, Silicon Catalyst is partnering with Intermolecular, the Silicon Valley science hub of Merck KGaA, Darmstadt, Germany and its electronics business which operates as EMD Electronics in the U.S. and Canada. Through their Startup Accelerator program, Intermolecular engages the start-up ecosystem to offer R&D services and explore potential new applications. These can be in areas ranging from neuromorphic computing and architectures, quantum computing to sustainability, and semiconductors - any application where materials play a key role in product development.



DR. JACOB WOODRUFF
HEAD OF
TECHNOLOGY SCOUTING
AND PARTNERSHIPS

Dr. Jacob Woodruff is Head of Technology Scouting and Partnerships, NA and EU, with EMD Electronics, where he works to find and advance external early stage and disruptive technologies. Dr. Woodruff is an experienced technologist, having managed global R&D groups developing semiconductor deposition materials at EMD Electronics. Previously, he lead ALD process technology development teams at ASM, and at SunPower and Nanosolar, managed R&D labs and developed processes for solar cell manufacturing. He holds a Masters in Materials Science and Engineering and a PhD in Physical Chemistry from Stanford University.

SILICON STARTUP SOLUTIONS

"As our science hub in the Silicon Valley, Intermolecular acts as a valuable toolbox of integral research, testing, and development capabilities that allow us to continuously advance material innovation," said Jacob Woodruff, Head of Technology Scouting & Partnerships, EMD Electronics

"Intermolecular's custom-built tools, test vehicles, and rigorous analytics, coupled with tailored methodologies enable IP-protected, high-quality data generation for accelerating materials, processes, and device learnings," added Ganesh Panaman, Head of Intermolecular.

Intermolecular is the trusted partner in materials innovation and can work with startups to help accelerate the speed of learning and generate datasets for AI/ML through its full suite of innovation services. These include screening materials to identify which ones will work best for the startup's goals, exploring multiple materials for a given application, studying materials companies are most interested in, and delivering solutions to customers' specifications.

Additionally, Intermolecular's proven workflows and simplified test vehicles can be deployed to physically, optically, and electrically characterize individual films and film stacks and understand their impact on device performance. The result is demonstrated high-quality and comprehensive data sets that customers leverage to make confident material decisions that lead to smarter product development.

Whether it is achieving a proof-of-principle, a first prototype, or a small series production, Intermolecular tailors solutions to meet a startup's unique needs.

ABOUT EMD ELECTRONICS

EMD Electronics is the U.S. and Canada electronics business of Merck KGaA, Darmstadt, Germany. EMD Electronics' portfolio covers a broad range of products and solutions, including high-tech materials and solutions for the semiconductor industry as well as liquid crystals and OLED materials for displays and effect pigments for coatings and cosmetics. Today, EMD Electronics has approximately 2,000 employees around the country, with regional offices in Tempe (AZ) and Philadelphia (PA). For more information, please visit www.emd-electronics.com.

ABOUT INTERMOLECULAR

Intermolecular is a trusted partner for materials innovation and the Silicon Valley science hub of Merck KGaA, Darmstadt, Germany and its electronics business. Intermolecular explores, tests and develops advanced materials that are revolutionizing the next generation of electronics that make lives easier, entertaining and more productive. For more than 15 years, the team, methodologies and quality data have driven impactful outcomes, market opportunities and innovative product designs for customers.

Reach out to us at jacob.woodruff@emdgroup.com to learn how we can accelerate the discovery and development of your products.

IN-KIND PARTNER NEWS
MATHWORKS

6G's Goals and Requirements are Coming into Focus

by Houman Zarrinkoub, Ph.D., Principal Wireless Product Manager, MathWorks

Every wireless standard is built with specific goals to drive the industry forward. 4G focused on flexible IP-centric voice, data, and video communications. 6G is envisioned to provide more ubiquitous, efficient, and immersive wireless connectivity. As research and development for 6G systems are ongoing, we're seeing tremendous breakthrough work taking place within the startup ecosystem as seen with Silicon Catalyst-supported firms.

MathWorks is supporting the 6G development in a number of ways, including providing free software and technical support through our Accelerator Partnership with Silicon Catalyst and our Suites for Startups program providing a multi-year program allowing the startups to progress from Concept to MVP to Production.

Here's an in-depth look at the enabling technologies wireless engineers should begin to account for in their current and future projects.

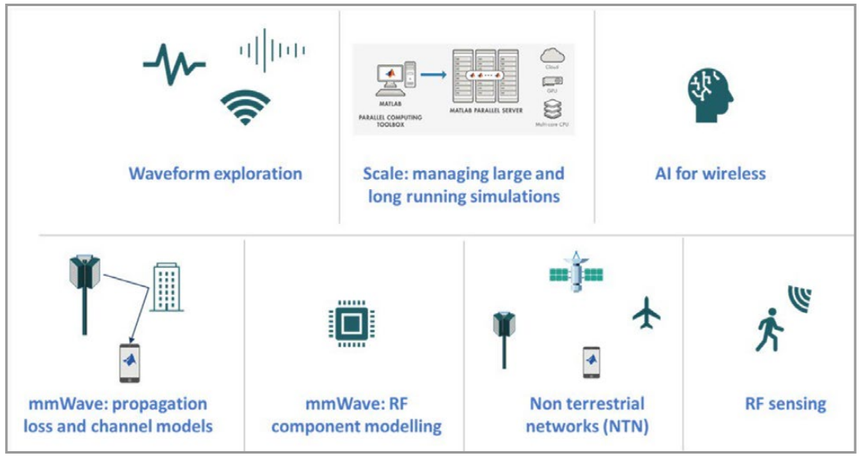
NEW FREQUENCIES, INCLUDING SUB-THZ COMMUNICATION

The use of new frequencies in range (from 7-24 GHz) and Sub-THz range (larger than 100 GHz) will most likely be part of the 6G communications systems. This will enable new spectrum management methodologies and deliver performance gains in data rate and speed, augmenting network capacity and transmission bandwidths while reducing network interference.

JOINT COMMUNICATION AND SENSING

Future wireless networks need to accurately localize wireless devices to optimize their transmissions. By introducing new frequencies, wireless networks can furnish highly accurate sensing and yield spatial knowledge of their physical surroundings. This is why 6G will use joint communication and sensing (JCAS) that integrates a wireless network's localization, sensing, and communication functions.

JCAS systems can improve performance in indoor communications scenarios by acquiring and sending better information about the indoor space, range, barriers, and positioning to the network. According to recent research from Ericsson, one of JCAS' primary benefits is that "most of the infrastructure is already in place with transmit/receive (Tx/Rx) nodes providing full area coverage as well as a good interconnection between nodes, which facilitates a multi-static sensory mesh." If sensing is already integrated into wireless systems, 6G's introduction of new frequencies in the sub-THz spectrum may pave the way for wireless engineers to use radar-like technologies. However, the challenge in designing a JCAS system is the increased computational complexity of the combined systems, and the resulting competition for the available resources, can slow down or disrupt wireless service.



The 6G wireless communications workflow will include AI, non-terrestrial networks (NTNs), waveform exploration, mmWaves, and enhanced RF sensing.

DR. HOUMAN ZARRINKOUB

PRINCIPAL PRODUCT MANAGER, MATHWORKS

Dr. Houman Zarrinkoub is the principal product manager at MathWorks responsible for wireless communications products. During his 22-year tenure at MathWorks, he has also served as a development manager and has been responsible for multiple signal processing and communications software tools. Prior to MathWorks, he was a research scientist working on mobile and voice coding technologies in the Wireless Group at Nortel Networks. He has been awarded multiple patents on topics related to computer simulations of signal processing applications. Houman is the author of the book Understanding LTE with MATLAB: From Mathematical Modeling to Simulation and Prototyping. He holds a B.Sc. degree in electrical engineering from McGill University and M.Sc. and Ph.D. degrees in telecommunications from the University of Quebec, in Canada.

RECONFIGURABLE INTELLIGENT SURFACES

Reconfigurable intelligent surfaces (RIS) are gaining traction within the wireless community for their ease of deployment, spectral efficiency enhancements, compatibility with current wireless networks' standards and hardware, and sustainability. RIS is a new type of medium that allows engineers to control the propagation of signals between a transmitter and a receiver dynamically and programmatically through an array of reflecting elements. The ability to actively reflect and steer incoming signals off surfaces requires wireless engineers to use MIMO wireless systems that improve steerability but necessitate additional antennas and narrow beams. Narrow beams can be challenging because any small mistake in aiming the beam could prevent it from reaching its intended target.

All these types of innovations add a tremendous amount of complexity and variability to a wireless system and make the design space exploration task very difficult. Wireless engineers building these types of wireless systems frequently use MATLAB and Simulink to design, model, test, and analyze their designs. Engineers can explore new frequency ranges, bandwidths, numerologies, and scale simulations for MIMOs and higher sampling rates in a consequence-free simulated environment.

NON-TERRESTRIAL NETWORKS FOR WIRELESS CONNECTIVITY

A critical technological advancement in ubiquitous connectivity is the emergence of non-terrestrial networks (NTNs). NTNs are any network involving non-terrestrial flying objects, including low-earth-orbit (LEO) satellites. Wireless engineers have increasingly integrated mobile devices into terrestrial networks to create hybrid terrestrial/non-terrestrial 5G mobile infrastructures to serve enterprises and consumers. Apple's Emergency SOS feature is the most notable application. NTNs are valuable because they make building a global wireless network possible without relying on cellular towers, particularly in regions where construction isn't economically viable.

AI IS CRITICAL FOR 6G SYSTEMS

The increasing complexity of 6G networks necessitates the usage of AI. Designers can't realistically keep up with the enhanced speed and complexities introduced by 6G. AI techniques can solve non-linear problems by extracting underlying patterns automatically and efficiently, beyond the ability of human-based approaches.

Engineers can apply AI, including machine learning, deep learning, or reinforcement learning workflows, to configure, optimize, and self-organize 6G wireless communications. Further, 6G will likely support AI-based air interfaces to improve functions, such as joint compression and coding, beamforming, channel state information (CSI) compression, and positioning. AI can also benefit project management by incorporating simulated environments into an algorithmic model by estimating source environment behavior, enabling engineers to quickly study a system's dominant effect using minimal computational resources.

The best thing about wireless communications is that math and physics are never disputed. The problems arise from the requirements and technologies that make them viable and efficient. We don't know which candidate technologies will be included in the 6G standard until 2026, but wireless engineers should prepare themselves for upcoming innovations now. Wireless engineers that use AI to build designs incorporating JCAS, RIS, or NTNs and use simulations to test them will be much better positioned to execute once 6G's requirements are established.

Learn more about MATLAB & Simulink for wireless: Wireless, 5G Toolbox, 6G, AI for Wireless
Learn more about MathWorks Startup Program: MATLAB for Startups, MATLAB Startup BLOG

IN-KIND PARTNER
COVALENT METROLOGY

Covalent Metrology Joins the Silicon Catalyst In-Kind Partner Ecosystem

Silicon Valley, California, May 31, 2023 – Silicon Catalyst, an incubator exclusively focused on accelerating semiconductor solutions, announced that Covalent Metrology has joined as a new member of its In-Kind Partner ecosystem. Covalent Metrology, a leading provider of premier analytical services in North America, joins Silicon Catalyst to offer the incubating Portfolio Companies a full suite of modern semiconductor analysis capabilities, fueling their implementation of a more comprehensive and deliberate metrology strategy.

As recent public policy spurs the domestication of semiconductor fabrication and development, small companies and start-ups may need a revamped data strategy to stay competitive. This partnership connects Silicon Catalyst's portfolio companies to Covalent's comprehensive semiconductor metrology solutions, making critical insights more affordable and accessible.

Since its founding, Covalent Metrology has worked with a wide variety of semiconductor customers across many areas of product development: providing advanced microscopy, surface analysis, x-ray metrology, and analytical chemistry services from the supply chain to the fab. Covalent's $20M laboratory is headquartered in the heart of Silicon Valley, and hosts showcase rooms for strategic partners: all global leaders in advanced scientific instrumentation. Through these partnerships, Covalent clients can access the latest metrology capabilities on state-of-the-art analytical tools operated by metrology and semiconductor experts. This unique combination of deep domain expertise, extensive applications experience in the industry, and a next-generation lab outfit enable Covalent to deliver exclusive solutions for semiconductor products.

Covalent Brings 100+ Modern Semiconductor Metrology Techniques to the Incubator's Network to Empower Next-generation Start-ups

"Innovation in the semiconductor ecosystem is alive and well, and increasingly flourishing in the United States," states Craig Hunter, Chief Executive Officer at Covalent Metrology, "Silicon Catalyst has done an incredible job of building a vibrant semiconductor start-up community based right here in Silicon Valley. We are very much looking forward to a closer collaboration with the exciting family of companies at Silicon Catalyst."

Silicon Catalyst has developed an unparalleled support ecosystem for its semiconductor start-ups, providing a strong network of financiers, business advisors, and industry professionals who help companies to launch and scale in the market. In addition, the incubator provides privileged access to services, expertise, and intellectual property that can empower their companies' technological innovation. Dr. Atiye Bayman, Partner at Silicon Catalyst, stated, "To best serve semiconductor start-ups, Silicon Catalyst works relentlessly to expand our ecosystem with top talent and new capabilities. Covalent Metrology is a welcome addition to our In-Kind Partner Program, as they bring exclusive capabilities and modern, advanced metrology solutions for semiconductor research. Our Portfolio Companies should never have to compromise in getting what they need to be successful. Covalent can support them in implementing a more robust characterization strategy."

ABOUT COVALENT:

Covalent Metrology is a disruptive analytical services laboratory and digital platform based in Sunnyvale, California. Its mission is to empower technological innovation with superior data and insights. Covalent makes it easier and more affordable to access the metrology data necessary for strategic decision-making: facilitating faster research, development, and production of advanced materials and devices. It is dramatically changing the materials characterization service landscape with the combination of its modern data platform, world-class analysts and top-notch customer service, state-of-the-art analysis instrumentation, and strategic partnerships. Covalent now has over 500 customers in 30+ industries. Learn more at: https://covalentmetrology.com.

IN-KIND PARTNER
COLLIERS

Colliers Joins Silicon Catalyst Ecosystem as an In-Kind Partner

Silicon Valley, California, May 18, 2023 – The Silicon Valley office of Colliers announced today that it has joined Silicon Catalyst, the world's only incubator focused on accelerating semiconductor solutions, as an In-Kind Partner.

Colliers provides commercial real estate professional and investment management services to corporate and institutional clients in the Americas, Europe, the Middle East, Africa, and the Asia-Pacific region. Portfolio Companies in the Silicon Catalyst incubator will be able to utilize the real estate services of Colliers to find appropriate office and lab facilities to enable their further business growth.

Brokers Jere Hench and John McMahon, both of whom are Executive Vice Presidents in the Silicon Valley office of Colliers, have spent their careers providing services to these types of companies.

"Our work with early-stage companies has intersected with Silicon Catalyst's in the past and it's exciting to be working alongside them now in an official capacity. While these companies grow, it's critical that we help them make the best real estate decisions as they scale," Hench said.

"It's very important that the Silicon Catalyst In-Kind Partner ecosystem continues to address the needs of the early-stage companies in our incubator. As they achieve success in the market, it's great to know that they'll be able to leverage Colliers' expertise to address their facility needs," stated Tarun Verma, Silicon Catalyst Managing Partner.

JERE HENCH
BROKER

JOHN MCMAHON
BROKER

ABOUT COLLIERS:

Colliers is a leading diversified professional services and investment management company. With operations in 63 countries, our 18,000 enterprising professionals work collaboratively to provide expert real estate and investment advice to clients. With annual revenues of $4.6 billion and $92 billion of assets under management, Colliers maximizes the potential of property and real assets to accelerate the success of our clients. Learn more at corporate.colliers.com, Twitter @Colliers or LinkedIn.

ABOUT SILICON CATALYST:

"It's about what's next"

Silicon Catalyst is the world's only incubator focused exclusively on accelerating semiconductor solutions, built on a comprehensive coalition of in-kind and strategic partners to dramatically reduce the cost and complexity of development. More than 900 startup companies worldwide have engaged with Silicon Catalyst and the company has admitted 97 exciting companies. With a world-class network of mentors to advise startups, Silicon Catalyst is helping new semiconductor companies address the challenges in moving from idea to realization. The incubator/accelerator supplies startups with access to design tools, silicon devices, networking, and a path to funding, banking and marketing acumen to successfully launch and grow their companies' novel technology solutions. Over the past eight years, the Silicon Catalyst model has proven to dramatically accelerate a startup's trajectory while at the same time de-risking the equation for investors. Silicon Catalyst has been named the Semiconductor Review's 2021 Top-10 Solutions Company award winner.

The Silicon Catalyst Angels was established in July 2019 as a separate organization to provide access to seed and Series A funding for Silicon Catalyst portfolio companies.

More information is available at www.siliconcatalyst.uk, www.siliconcatalyst.com and www.siliconcatalystangels.com.

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Richard Curtin
Managing Partner

Portfolio Companies

CURRENT

Liitto

weeteq

veevx

Cambridge TERAHERTZ

ABR

NIOBIUM MICROSYSTEMS

EXOKERYX

POLYN TECHNOLOGY
NEUROMORPHIC ANALOG SIGNAL PROCESSING

XCELERIUM

QPT

ZEPSOR TECHNOLOGIES

cellsemi

KURA

Siloxit

Lemurian Labs

RAAAM
The Highest Density On-Chip Memory in Standard CMOS

plife BIOTECH

NanoHydroChem
Energy Storage Solutions

PHINOMICS

Lelantos

MultiFractal SEMICONDUCTORS

SigmaSense

ESPRE TECHNOLOGIES

MENTIUM TECHNOLOGIES

GEEGAH

PORTFOLIO COMPANY NEWS

Silicon Catalyst Announces Four Newly Admitted Companies to Semiconductor Incubator

Silicon Valley, CA, and London, England - June 7, 2023 – Silicon Catalyst, the world's only incubator focused exclusively on accelerating semiconductor solutions, announces the admission of four companies into the semiconductor industry's highly acclaimed program.

The newly admitted companies include:

CAMBRIDGE TERAHERTZ
Democratizing the Terahertz spectrum through CMOS phased array technology

LIITTO
Computing Solutions for the Clean Energy Era

VEEVX
Intelligent Memory Chiplets

weeteq
The "tiny" embedded technology company

Silicon Catalyst has developed an unparalleled support ecosystem for its semiconductor start-ups, providing a strong network of Strategic Partners, technical & business advisors, and industry professionals who help companies to launch and scale in the market. In addition, the incubator's In-Kind Partners provide privileged access to services, expertise, and intellectual property that can help commercialize their companies' technological innovation.

"Our most recent applicant screening cycle was truly spectacular, with a record number of entrepreneurial teams from 14 countries looking to participate in our 24-month incubation program," stated Paul Pickering, Managing Partner at Silicon Catalyst. "These four companies exemplify our mission to assist in building out the next generation of semiconductor-based solutions to address the significant market challenges and opportunities in the areas of communications, energy, IoT and embedded systems."

Cambridge TERAHERTZ

Utilizing the Terahertz spectrum to save and improve lives on a global scale
Cambridge Terahertz was spun out of MIT in 2021 with the mission to bring Terahertz technology to the world. Our Terahertz CMOS phased array technology is setting orders-of-magnitude performance records, enabling low-cost and widely deployed Terahertz wireless systems, unlocking the benefits of this untapped frequency range. The list of impactful/lucrative markets for such a tech is extremely long but we are beginning with imaging, starting with the physical security and loss prevention markets. We're building a future where detection of weapons and contraband is ubiquitous and blends into the background.

Liitto

Computing Solutions for the Clean Energy Era
Liitto builds hardware that transforms low-priced and wasted clean energy into a valuable computational resource. Our unique solution helps solar and wind power plants address the $11 billion annual problem of value deflation and curtailment. Simultaneously, we provide a path to decarbonize the fast-growing, energy-intensive fields of computation, ranging from Bitcoin Mining to AI Training.

veevx

Intelligent Memory Chiplets
Veevx Intelligent Memory (iRAM) Chiplets combine high performance, high density, and ultra-low power enabling the next generation in memory technology to service the demands from a wide variety of markets. iRAM performance and non-volatility enables replacement of large block SRAM with 100X reduction in deep sleep power and 2X improvement in density. The Veevx Intelligent Memory product family spans memory densities from 2MB to 128MB and supports 3D and 2.5D packaging options with a configurable Chiplets interface.

weeteq

The 'tiny' embedded technology company
weeteq is pioneering a new approach to circuit design for industrial applications, optimizing operational performance and unsupervised machine learning, for every closed-loop control system, changing the way industries approach digital transformation. Ultra Edge® technology introduces circuit-level artificial intelligence, which solves real-world industrial-scale challenges, reducing cost and energy expenditure, whilst increasing productivity and uptime of assets. Our goal is for our 'tiny', embedded technology to become a ubiquitous presence within the circuits and components of Industry 4.0 solutions.

PORTFOLIO COMPANY NEWS
SIGMASENSE

SigmaSense teams up with NXP to transform touch interfaces

by Dean Takahashi I May 16, 2023 | venturebeat.com

SigmaSense announced a license and co-development deal with NXP Semiconductors to create a new kind of multi-dimensional sensing technology to revolutionize user experiences.

Austin, Texas-based SigmaSense has licensed technology to NXP, and the companies will collaborate on high-performance sensing products for specific applications with demands for faster, more robust, fully immersive software-defined experiences.

NXP recently said it invested $35 million in the first tranche of a SigmaSense Series B funding.

“The next generation of smart devices and applications are demanding data for enhanced functionality that requires an entirely new software-programmable approach to sensing,” said Lars Reger, CTO of NXP Semiconductors, in a statement. “SigmaSense created a breakthrough in sensing technology with an innovative approach that makes exciting new product designs possible. We are thrilled to team with SigmaSense to productize a new era of NXP solutions.”
SigmaSense innovations make it possible to extract vastly more data from the physical world for a wide range of products and systems. Multi-dimensional sensing works through many different surfaces, shapes, and materials, enabling previously impossible designs.

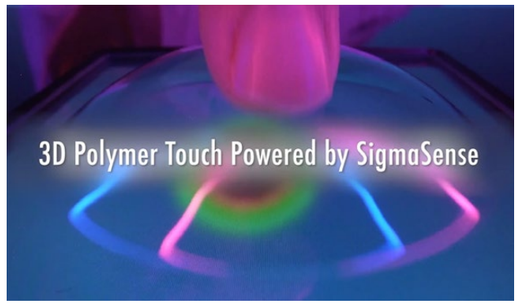
“NXP’s prowess in highly dependable products and deep expertise in high-volume semiconductor design combined with SigmaSense technology will accelerate game-changing sensing products,” said Rick Seger, CEO of SigmaSense, in a statement. “Our co-development with NXP marks the transition to a universe of new data-centric design options driven by software-defined sensing.”

With the invention of measuring current direct-to-digital, SigmaSense delivers low-voltage, frequency domain sensing, an industry first. Fast, continuous, high-fidelity data capture with intelligent digital signal processing moves analog challenges to the digital domain, where design

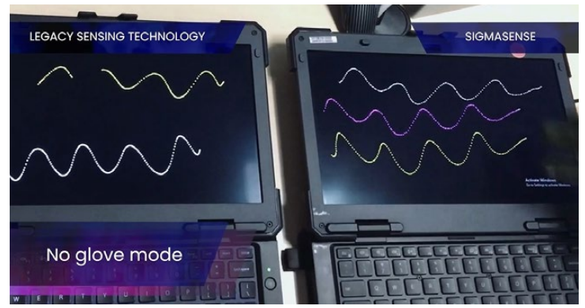
SILICON STARTUP SOLUTIONS

PORTFOLIO COMPANY NEWS
SIGMASENSE

SigmaSense teams up with NXP (cont’d)



SigmaSense powers a 3D polymer touch technology.



SigmaSense has high-performance and low-power touch technology.

flexibility can deliver orders of magnitude improvement.

SigmaSense is changing system designs from foldable displays to EV batteries.

Founded in 2016, SigmaSense invented a foundational technology that transforms the interactions between digital systems and the physical world, ushering in a new era of radically enhanced digital sensing. SigmaSense software-defined sensing achieves breakthrough levels of speed, accuracy, resolution, and noise immunity previously deemed impossible for sensing systems. The company has 70 people and it has raised $93 million to date.

Asked what the inspiration for the company was, Seger said in an email to GamesBeat, “The SigmaSense founders have deep roots in the touch and tablet industry with the pioneering companies Wacom and N-trig, which was acquired by Microsoft in 2015. In looking to the future horizon, the founders turned their attention to examining how to change sensing for the better across a number of markets. The vision included a particular interest in enabling superior pen and touch to serve education with the benefits of pervasive access to writing captured digitally. As it turned out the team’s R&D efforts delivered a step change improvement in the sensing system to serve new requirements for superior data from high-performance processing systems.”

Sensing through the noise, SigmaSense products increase the depth and quantity of data that can be captured from the physical world to enable exciting new experiences in a wide range of devices including mobile, automotive, battery sensing, digital signage, wearables, and all sizes of IoT touch displays. SigmaSense is funded by strategic investors, including NXP, Foxconn, LG-MRI, E ink, Corning, and GIS.

Asked about the significance of the tech, Seger said, “All systems are based on a cycle of sense, process, and react that forms the user experience. The key is how fast the cycle can occur with high-quality data. Today, the quality and speed of data extraction from the physical world is becoming as important, if not more important than processing performance. The extraction of deep, high-quality data opens new markets and accelerates innovation for HMI products. Significantly, the shift from fixed analog device sensing to software-defined sensing offers greater programmability and flexibility essential for innovation.”

Seger noted that examples include gameboards with 3D sensing, object recognition, and multiple player ID of who is touching at high-performance speeds. No amount of processing power can achieve the speed requirements of the sense, process, and react cycle if it cannot extract the sensed information at an equally high speed, he said.

He also said that, for batteries, the tech would create the ability to detect and avoid thermal runaway by measuring the impedance of the battery providing better-informed state of charge, and state of health information. And he said that we’ll see foldable mobile device experiences, with high performance and reliable touch with thinner materials, operation in the rain, and snow, and with gloves.

PORTFOLIO COMPANY NEWS
APPLIED BRAIN RESEARCH

ABR

CEO Interview: Dr. Chris Eliasmith and Peter Suma, of Applied Brain Research Inc.

by Daniel Nenni I January 6, 2023 I SemiWiki.com

Professor Chris Eliasmith (right side) is co-CEO and President of Applied Brain Research Inc. Chris is also the co-inventor of the Neural Engineering Framework (NEF), the Nengo neural development environment, and the Semantic Pointer Architecture, all of which are dedicated to leveraging our understanding of the brain to advance AI efficiency and scale. His team has developed Spaun, the world's largest functional brain simulation. He won the prestigious 2015 NSERC Polanyi Award for this research. Chris has published two books, over 120 journal articles and patents, and holds the Canada Research Chair in Theoretical Neuroscience. He is jointly appointed in the Philosophy, Systems Design Engineering faculties, as well being cross-appointed to Computer Science. Chris has a Erdős–Bacon number of 8.

DR. CHRIS ELIASMITH CEO, DIRECTOR, AND CO-FOUNDER

Peter Suma (left) is a co-CEO of Applied Brain Research Inc. Prior to ABR, Peter led start-ups in robotics and financial services as well as managed two seed venture capital funds. Peter holds degrees in systems engineering, science, law and business.

WHAT IS ABR'S VISION?

ABR's vision is to empower the world's devices with intelligent, concept-level conversations and decision-making abilities using our innovative Time Series Processor (TSP – appliedbrainresearch.com/products/tsp/) chips.

Whether it's enabling full voice and language processing on a small, low-power chip for consumer electronics and automotive applications, processing radar signals faster and for less power, bringing cloud-sized AI signal processing on to devices, or integrating situational awareness AI to give robots the ability to understand and respond to complex commands to interact with people in a natural and intuitive way, our TSP chip family is poised to revolutionize the way devices sense and communicate.

ABR has been delivering advanced AI R&D projects since 2012 to clients including the US DoD, Intel, BMW, Google, Sony and BP. Some examples of our work include, developing the world's largest functional brain simulation, building autonomous drone controllers for the US Air Force, and building small, powerful voice control systems for cars, appliances and IoT devices. Our TSP chips are our latest innovation as we work to fit more and better AI models into devices to give devices better artificial 'brains'.

HOW DID ABR BEGIN?

ABR was founded out of Dr. Chris Eliasmith's lab at the Centre for Theoretical Neuroscience at the University of Waterloo. Applied Brain Research Inc. (ABR) is now a leading brain-inspired AI engineering firm. Our AI engineers and neuroscientists develop technologies to improve AI inspired by work in AI and brain research at the lab.

PETER SUMA CHAIR OF THE BOARD OF DIRECTORS AND CO-FOUNDER

SILICON STARTUP SOLUTIONS

> Cameras, appliances, wearables, hearables, robots, and cars can all carry on complex, real-time, full language dialog with their users.

YOU MENTIONED YOU HAVE SOME RECENT DEVELOPMENTS TO SHARE. WHAT ARE THEY?

We are very excited to announce that ABR has been admitted to the ventureLab and Silicon Catalyst Incubator programs to support the development of our new Time Series Processor (TSP) family of edge AI chips, which allow cloud-sized speech and signal AI models to run at the edge at low cost, power, and latency. We will be exhibiting at CES in the Canada-Ontario Booth in the Venetian Expo Hall D at booth number 55429 from Jan 5th to Jan 8th, 2023, in Las Vegas. ABR is also a CES Innovation Awards Honoree (https://appliedbrainresearch.com/press/2022-11-21-ces-innovation-awards/) this year.

TELL US ABOUT THESE NEW CHIPS YOU ARE BUILDING?

Most electronic devices already do, or will soon have to, utilize AI to keep pace with the smart features in their markets. More powerful AI networks are larger AI networks. Today's edge processors are too small to run large enough AI models to deliver the latest possible features, and CPUs and GPUs are too expensive for many electronic devices. Cloud AI is also expensive, and for many products connections cannot be guaranteed to be accessible and are often not configured correctly by the customer.

What device makers need is a small, inexpensive, low-power chip that can run large AI models to enable the products to lead their respective markets. A very efficient, economical, and low-power way to achieve this is to compress large AI models and design a computer chip that runs these compressed models.

ABR has done exactly this with a new patented AI time-series compression algorithm called the Legendre Memory Unit or LMU. With this compression algorithm we have developed a family of small but very powerful time series processing AI processors that run speech, language and signal inference AI models in devices that previously would have required a cloud server.

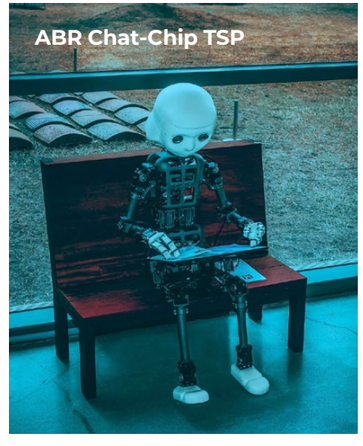
This enables more powerful and smarter devices with low power consumption. Batteries last longer, devices converse in full natural language sentences, and sensors process more events with greater accuracy. ABR is enabling a new generation of intelligent devices with our revolutionary low-power, low-cost and low-latency powerful AI Time Series Processor (TSP) for AI speech, language and signal processing.

WHAT ARE THE CHIPS IN THE ABR TSP FAMILY?

There are currently two chips in the ABR TSP family. The Chat-Chip TSP and the Signal-TSP.

The ABR Chat-Chip TSP is the world's first all-in-one full voice dialog interface, low-power chip. Low-cost and low-power speech chips until now have been limited to keyword-spotting AI models which are limited to understanding 50 or so words. These chips deliver those oh-so-frustrating speech interfaces in cars, toys and other speech-enabled, sometimes-disconnected, low-BOM-cost devices. ABR's Chat- Chip TSP replaces those chips for the same cost with a full natural language experience. Dramatically upgrading the customer's experience.

The ABR Chat-Chip enables a full natural language voice assistant in one chip, including noise filtering, speech recognition (ASR), natural language processing (NLP), dialog management, and text-to-speech (TTS) AI. The ABR Chat-Chip TSP can run cloud-sized speech and language AI models in one chip, consuming less than 50 milli-watts of power. This combination of low-cost, low-power and large speech and language AI model processing means the ABR Chat-Chip TSP brings full Alexa-like natural language dialog to all devices including devices that, until now, could never have implemented full language dialog systems due to cost, latency and model size limitations when using existing chips.



Cameras, appliances, wearables, hearables, robots, and cars can all carry on complex, real-time, full language dialog with their users. People can hear better with larger de-noising and attention-focusing AI models in earpieces. People can interact with

PORTFOLIO COMPANY NEWS
APPLIED BRAIN RESEARCH CONT.

CEO Interview cont'd: Dr. Chris Eliasmith and Peter Suma

devices, more privately, instantly, and more hygienically without touching buttons. The many robots in our lives now and the near future can interact verbally without a cloud connection. Devices can also explain to users how to use them, offer verbal troubleshooting, deliver their user manuals verbally, offer hygienic, touchless interfaces, handsfree operation, and market their features to consumers. All of this without needing an internet connection, but able to take advantage of one if present. Voice interfaces delivered locally are more private, as they do not send sound recordings to the cloud, eliminating the risk of leaking background noise and emotional context. As well, local dialog processing is faster, without the latency of a cloud network. Local dialog processing reduces device makers' costs per device and in the cloud, by removing large portions of the cloud processing needed for voice interfaces and performing the local processing at up to 10x less in-device processor cost.

The ABR Signal-TSP performs AI signal pattern and anomaly detection by running larger AI models, faster and for less power than existing CPUs and GPUs. In a market where larger AI models are typically much more accurate AI models, device makers need inexpensive, low-power, large AI model processors to make their devices smarter than the competition's. ABR's Time Series Processors (TSPs) cost just few dollars but run large AI models that otherwise would require a full CPU or GPU costing between $30 to $200 USD to execute the same workload in real-time. ABR's Signal TSP typically reduces power consumption by 100x, latency by 10x and cost by 10x over functionally equivalent CPUs or GPUs.

HOW ARE THE TSP CHIPS PROGRAMMED?

ABR supports the TSP chips with an API and an AI hardware deployment SaaS platform called NengoEdge (edge.nengo.ai). AI models can be imported from TensorFlow and then optimized for deployment to the TSP and other chips using NengoEdge. With NengoEdge you can pick a network, set various hardware-aware optimizations, and then have NengoEdge train and optimize the network using hardware specific optimizations, including quantization and utilization of any available AI acceleration features, such as the LMU fabric if a TSP is targeted. The result is an optimal packing of the AI network onto the targeted chips to deliver the fastest, lowest-power and most economical solution for delivering the chosen network onto the target hardware. All without buying each chip to test or learning the details of each chip. Users can see the TSP shine on all time series workloads, for example for voice assistants or radar processing AI systems.

CAN YOU TELL US MORE ABOUT YOUR LMU COMPRESSION ALGORITHM?

The Legendre Memory Unit (LMU) was engineered by emulating the algorithm used by time cells in the human brain and specifically how time cells are so efficient at learning and identifying event sequences. The LMU makes the ABR TSP's large gains in efficiency, performance and cost possible for inferencing all time series and sequence-based AI models. We patented the LMU worldwide in 2019 and announced it NeurIPS in December 2019. We then published the software versions of the LMU on our website and GitHub in 2020. There are many papers now published using the LMU and achieving state of the art results on time series workloads by other groups. We have many clients who have licensed the LMU software running on CPUs, GPUs or MCUs for signal and speech processing in devices such as wearables, medical devices and drone controllers. Many of those are now waiting to move to a TSP chip to extend their battery life and support even larger models at lower power, cost and latency levels.

WHEN WILL THE TSP CHIPS BE AVAILABLE?

We are working to have first silicon TSP chips for both the Chat-Chip and Signal design available by Q1 2024. We are signing pre-orders and design LOI's now. Contact Peter Suma, co-CEO of ABR at peter.suma@appliedbrainresearch.com or on 1-416-505-8973 to learn how we can super charge your devices to be the smartest in their class.

Portfolio Companies

ALUMNI

Trameto (Smarter EH PMICs)
ALPHA ICs (ADVANCING AI COMPUTE)
SALIENCE LABS
SONICAL
oculi
MEMTECH
beam
mmTron (Unleashing the mmWave Frontier)
quadric
DOVER MICROSYSTEMS
ERIDAN
OWL (AUTONOMOUS IMAGING)
AyarLabs
AEPONYX™
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Leveraging optical chip-to-chip connectivity to unleash the complete potential of AI – An interview with Ayar Labs

May 17, 2023 | www.yolegroup.com

Co-packaged optics (CPO) has gained attention recently due to its power efficiency in datacenters. While most leading proponents of CPO targeting networking applications have discontinued CPO programs due to macroeconomic headwinds, the situation of CPO for artifical Intelligence (AI) and machine learning (ML) systems is different. AI models have an insatiable demand for computing power, storage, and data movement, and traditional architectures are becoming the main bottleneck for scaling ML. As a result, new optical interconnects have emerged for HPC and new disaggregated system architectures, which Yole Intelligence, part of Yole Group **reviews in its new report,** Co-packaged Optics for Datacenter**. In-package optical I/O technology for xPUs, memory, and storage can help achieve the necessary bandwidths. Moreover, the potential for billions of optical interconnects in the future is driving big foundries to prepare for mass production (including silicon photonics process flows) of any PIC architecture from design houses. CPO revenue was about US$38 million in 2022 and is expected to reach US$2.6 billion in 2033, at a 46% CAGR for 2022 – 2033, driven by accelerated data movement in AI/ML gear.**

TERRY THORN
VICE PRESIDENT OF COMMERCIAL OPERATIONS

Terry Thorn is Vice President of Commercial Operations. He joined Ayar Labs after 24 years at Intel Corporation where he held a variety of leadership positions in product line management, marketing, global cloud strategy, new business development and sales. Most recently, Terry was the GM of Global Accounts in the Cloud & Enterprise Sales Group with direct ownership of some of Intel's largest customers. He has a Bachelor of Science in Mechanical Engineering and an MBA from the University of Alabama.

MARTIN VALLO
SENIOR ANALYST PHOTONICS AND LIGHTING

With 12 years' experience within semiconductor technology, Martin is involved today in the development of technology & market reports as well as the production of custom consulting projects at Yole. Prior to his mission at Yole, he worked at CEA (Grenoble, France), with a mission focused on the epitaxial growth of InGaN/GaN core-shell nanowire LEDs by MOCVD and their characterization for highly flexible photonic devices. Martin graduated from Academy of Sciences, Institute of Electrical Engineering (Slovakia) with an engineering degree in III-nitride semiconductors.

The combination of TeraPHY™ optical I/O chiplets and SuperNova™ light sources from Ayar Labs delivers dramatically increased bandwidth, at lower latency, over longer distances and at a fraction of the power of existing electrical I/O solutions. Its in-package optical I/O solution is disrupting the traditional performance, cost, and efficiency curves of the semiconductor and computing industries. Martin Vallo, Senior Analyst at Yole Intelligence, had the pleasure of interviewing Terry Thorn, Vice President of Commercial Operations at Ayar Labs, and discussing the current trends in optical interconnects for datacenter applications.

MARTIN VALLO (MV): We had our last interview in 2021 when you presented your breakthrough optical I/O solution enabling optical communication between computing chips. What is new in the life of Ayar Labs?

TERRY THORN (TT): Over the past 18 months, we have kicked off several high-profile strategic partnerships while also building key relationships with high-volume foundry, laser and supply chain partners. We started 2022 by celebrating a strategic partnership with Hewlett Packard Enterprise. Shortly thereafter, GlobalFoundries announced its new Fotonix manufacturing process that we used to demonstrate our first working silicon in June 2021 at OFC.

Other key milestones included our $130 Million Series C Funding, as well as partnerships with GPU and

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AYAR LABS CONT.

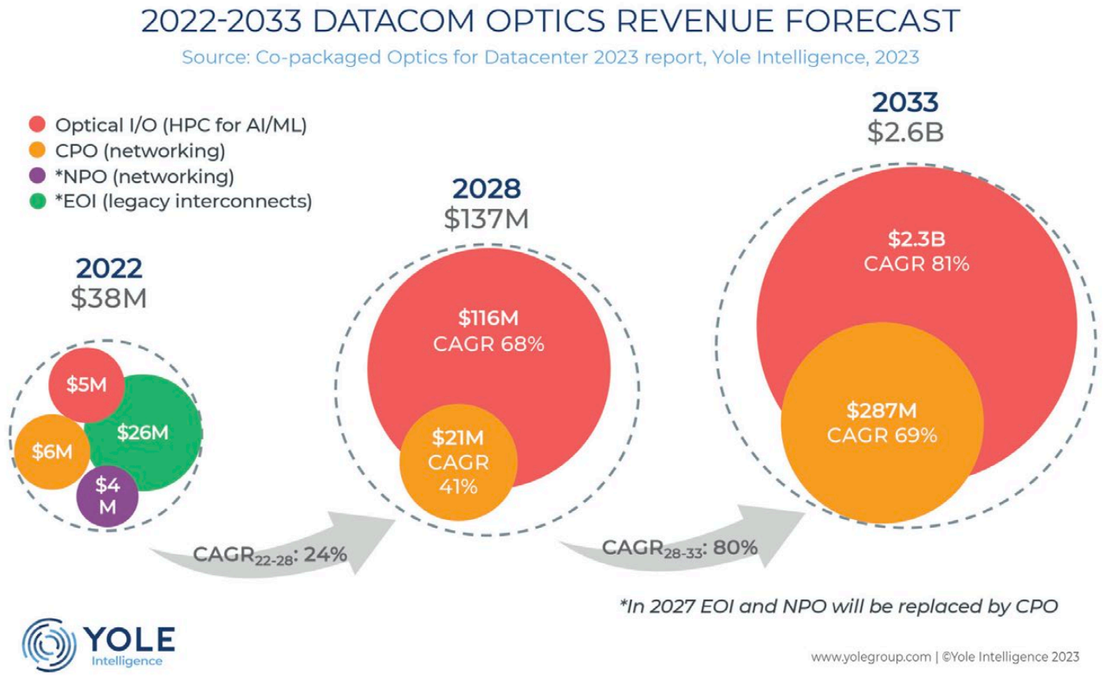
AI powerhouse NVIDIA and leading aerospace and defense contractor Lockheed Martin to develop optical interconnects. We closed out 2022 with the $15 million multi-year award of Project KANAGAWA with the Department of Defense that will promote the next-level development of Ayar Labs' optical interconnects to lead its transition into the DoD's advanced packaging ecosystem.

Most recently, we held a live demonstration of our optical I/O solution successfully showing 4 terabits per second (bidirectional) data transfer. We also featured our technologies in our ecosystem partners' booths, including GlobalFoundries, Quantifi Photonics and Sivers Photonics. The unveiling of a prototype of our solution with Intel's detachable optical connector at the package edge also generated a lot of interest at OFC this year. In a conventional edge-coupled method, the fiber ribbons are permanently attached into the V-grooves with epoxy. The detachable optical connector provides a means to replace the fiber ribbons. Still under development, the detachable optical connector holds promise for higher package yield and ease of field replacement.

We have also seen a growing trend towards using chiplets and a robust standardization effort to enable an open chiplet ecosystem. This is an important development that is aligned with our vision of delivering optical I/O solutions in the form of chiplets.

MV: WE OBSERVE THERE IS LESS INTEREST IN CPO, PARTICULARLY FOR SWITCH APPLICATIONS. HOWEVER, THE DEMAND FOR OPTICAL I/O FOR HIGH-PERFORMANCE COMPUTING CONTINUES. WHAT ARE THE UNDERLYING REASONS FOR THIS?

TT: Optical I/O is better suited for high-performance computing (HPC) and artificial intelligence (AI) / machine learning (ML) applications, where you need distributed computing and shared memory capacity to meet demands for performance, power and bandwidth without increasing latency. Optical I/O with wavelength division multiplexing (WDM) and simple modulation requires far less power and allows much greater density – as low as a few pJ/bit and a bandwidth density of up to 1 Tbps/mm – resulting in just a few nanoseconds of latency, versus



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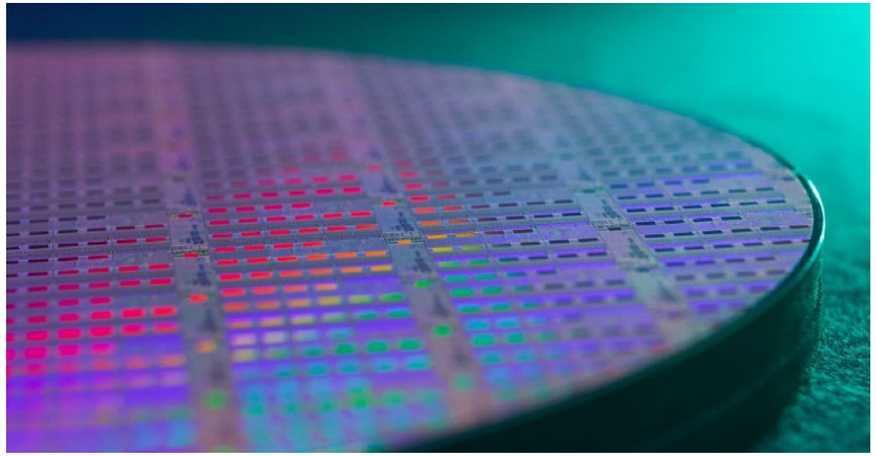

Ayar Labs TeraPHY™ optical I/O wafer from GlobalFoundries Fotonix™ monolithic RF-CMOS platform.

Courtesy of Ayar Labs, 2023

hundreds of nanoseconds with CPO that tends to use complex modulation schemes.

In addition, as an electro-optical transceiver, optical I/O uses a microring modulator structure, requiring a much smaller chip area that results in a lower cost. For example, our microring modulator is approximately one hundredth the size of a Mach-Zehnder modulator. Lastly, optical I/O uses WDM, which allows multiple data streams to be packed into a single fiber to achieve very high throughput.

MV: WHAT WILL BE THE FIRST ACTUAL APPLICATION FOR OPTICAL I/O, AND WHEN CAN WE EXPECT AN ANNOUNCEMENT? WHAT ARE THE CHALLENGES TO OVERCOME BEFORE WE SEE THE FIRST OPTICAL I/O IN AI/ML SYSTEMS?

TT: We see many different applications that are all running into the same power, performance, and latency challenges, and each has a strong need for optical I/O:

Artificial Intelligence and HPC. AI/ML and HPC applications require a distributed network of accelerators to disperse the computations and share memory capacity. With respect to memory capacity, an AI/ML model with hundreds of billions of parameters may require up to 2 terabytes of memory capacity to store intermediate computation results. When you connect hundreds of GPUs in a cluster such that every GPU can talk to the others, the data throughput required out of each GPU multiplies quickly. This puts enormous pressure on bandwidth density – a measure of data throughput that can be realized per package edge or area. Optical I/O is critical to achieve the required bandwidth density, power, and latency performance metrics to enable larger clusters.

High-Bandwidth Memory (HBM) Expanders. A GPU is typically surrounded by two to four local memory HBM stacks, each having about 64 GBytes of memory capacity. For HPC and AI/ML applications, this capacity is not sufficient. An HBM memory expander can be used to increase memory capacity to hundreds of GBytes and more. Since memory applications are very latency sensitive, using optical I/O links to connect the GPUs to the expander memory modules is necessary. Pluggable optics or CPO optics are not suitable due to the latency issue alone.

Memory Pooling and Composable Infrastructure. As cloud infrastructure deals with dynamically changing workloads, flexibility to pool and share memory is becoming critical. The vision of composing workload-based clusters with desired CPUs, GPU, memory and storage resources that are interconnected with high performance and low latency. Optical I/O interconnect is coming into focus with adoption of the CXL™ standard.

Sensory Systems for Aerospace and Defense. In this example, one that reflects our recently announced strategic collaboration with Lockheed Martin, optical I/O is used to capture, digitize, transport and process spectral information. Multi-chip package solutions that place high-density, high-efficiency optical I/O chiplets in the same package as the RF

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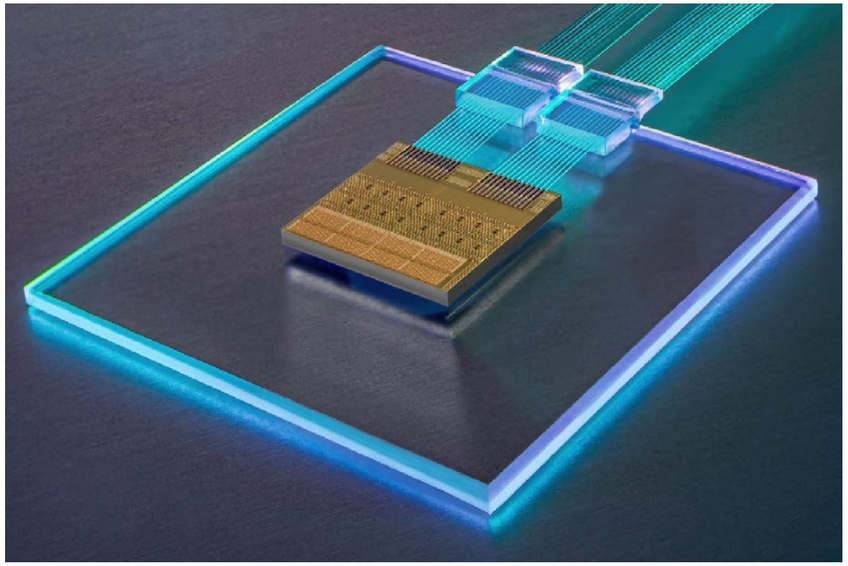

Ayar Labs TeraPHY™ optical I/O chiplet with 4 Tbps bi-directional bandwidth, at less than 5pJ/b, latency of 5ns per chiplet + TOF, and a reach of millimeters to kilometers.

Courtesy of Ayar Labs, 2023

processing devices will be used in phased-array apertures to connect systems to make smarter and faster decisions. Currently, the primary challenge for optical I/O is ecosystem development, which requires the coordination of many companies. We are working with a wide range of partners to foster the development of that ecosystem. As for the first announcements of these applications, we expect those to come sooner rather than later given the existing market need, perhaps within the next year or so.

MV: OPTICAL I/O PERFORMANCE ENABLES XPUS TO COMMUNICATE WITH EACH OTHER ACROSS A WIDE RANGE OF DISTANCES, FROM MILLIMETERS UP TO TWO KILOMETERS. THEREFORE, INTENSE COMPETITION IS EXPECTED BETWEEN AOC (ETHERNET) AND OPTICAL I/O (CXL, UCIE). HOW WILL THE BATTLE BETWEEN THESE TWO TECHNOLOGIES PLAY OUT?

TT: There is a clear distinction between Ethernet applications and compute or memory-centric applications, so we do not view AOC as a direct competitor. Within the compute or memory-centric interconnect protocols, Compute Express Link™ (CXL) and Universal Chiplet Interconnect Express™ (UCIe™) are complementary. CXL is a higher-layer protocol that traditionally runs on a PCIe physical layer. Recently, CXL has been expanded to also work with a UCIe physical layer. For off-chip connectivity within racks or across racks, UCIe optical retimers built using optical I/O technology can deliver low power, low latency, and high bandwidth density metrics that cannot be met with AOC.

With optical interconnects, we can achieve greater reach with lower power consumption and latency. There will still be non-latency-sensitive applications that can accommodate higher power requirements, and Ethernet will be the preferred choice, including system-to-system communications. In these instances, AOC could be used. But once you start considering deep learning and HPC application – where, again, you are connecting many compute nodes together – AOC may not meet all the performance metrics.

MV: HOW DO YOU SEE THE EVOLUTION OF OPTICAL I/O IN TERMS OF TECHNOLOGY?

TT: First and foremost, optical I/O is highly scalable and there are several ways the technology will evolve. One is in the number of lambdas per fiber. We are currently using eight lambdas per fiber, but the CW-WDM MSA (Continuous-Wave Wavelength Division Multiplexing Multi-Source Agreement) roadmap already has specifications for 16 and 32 lambdas per fiber. Every time you double the number of lambdas per fiber – keeping everything else the same – you automatically double the amount of bandwidth. We can also scale up the number of optical ports (we are currently using eight) and increase the modulation rates (we are currently using a modulation rate of 32 Gbps).

Within optical I/O, we expect to see a divergence in the use of internal or external lasers. We continue to prefer the external laser approach given the compact form factor, flexibility, and field replaceability. We also believe UCIe is

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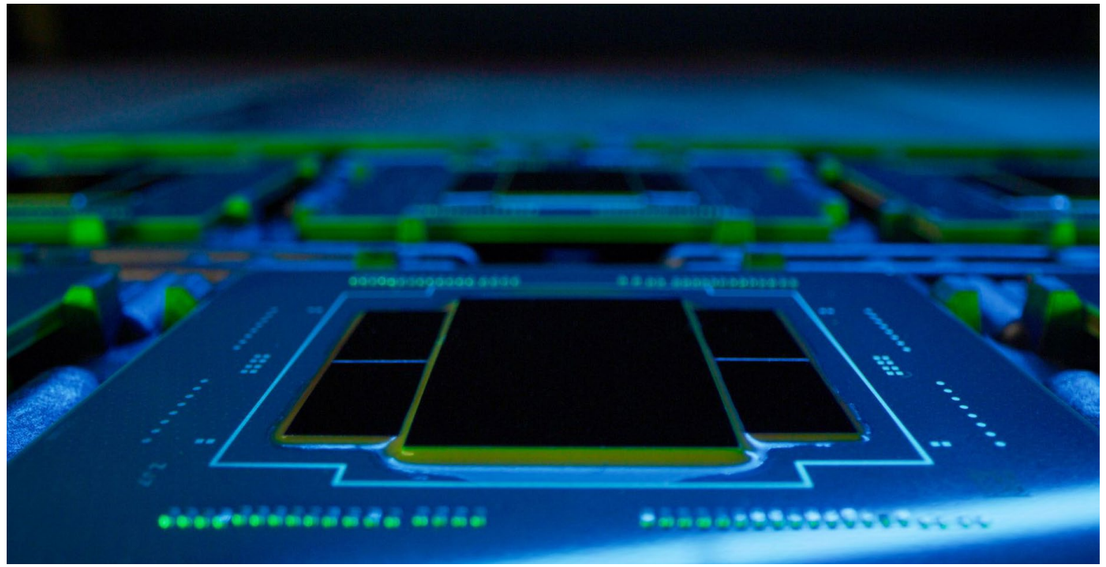

Four Ayar Labs TeraPHY™ optical I/O chiplets and a customer's ASIC in a multi-chip package.

Courtesy of Ayar Labs, 2023

the best-suited standard for die-to-die connectivity, which fosters the chiplet approach of implementing optical I/O.

MV: WHAT ARE THE KEY SPECIFICATIONS AROUND LASER SOURCES? WILL WE SEE WIDELY INTEGRATED LASERS IN OPTICAL CHIPLETS IN THE FUTURE?

TT: The current trend in the industry, and one we believe will continue, is the use of external laser sources. In optical I/O, the laser is the most sensitive component and needs to operate in a cooler temperature environment. Keeping it external and separate from the compute silicon allows you to better and more efficiently control the temperature. If you were to put the laser module next to the compute silicon, the heat coming from the GPUs and CPUs inside the compute node could impact the laser performance.

We do expect to see the use of comb lasers but they are still in the early research stage of development. It is something we could take a look at when the technology becomes commercially available. But, ultimately, we believe remaining 'external laser agnostic' makes the most sense in terms of manufacturing and deployment.

MV: THERE HAVE BEEN MANY DISCUSSIONS ON DISAGGREGATED RACK ARCHITECTURE, CURRENTLY THE MAIN DRIVER OF OPTICAL I/O TECHNOLOGY. COULD YOU SHARE HOW DISAGGREGATION WILL EVOLVE?

TT: Disaggregated infrastructure needs optical I/O to scale to the rack level and beyond. Disaggregated architectures that decouple memory from processors and accelerators allow for more flexible and cost-effective node designs that can meet the demands of next-generation HPC and AI workloads. For disaggregation to be possible, an interconnect that can deliver high throughput at low power and low latency over distances ranging from a few meters to hundreds of meters is critical. CXL, an emerging unified protocol for disaggregated systems, uses PCIe electrical signaling for I/O interconnect which has limited reach. To extend the reach and fanout, there is strong interest for a "CXL over optical" I/O interconnect.

For example, it is easy to envision a composability scenario in which several CPUs are contained in one chassis, and the GPUs are in a separate chassis while memory occupies another. As workloads scale up, you can compose two CPUs,

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one GPU, several SSDs and pool some amount of memory to create one node. CXL brings cache coherent interconnect to memory disaggregation, which is why so many companies are working towards solutions that leverage CXL – and we believe optical I/O is a key ingredient to enable that vision.

Another important angle here is distributed computing, which goes back to the fact that AI/ML and deep learning all require a massive amount of training parameters — now in the trillions. Sharing the computation and memory between various compute nodes will be increasingly necessary. The only reliable way to connect these nodes and scale efficiently is through optical I/O.

MV: BRINGING ELECTRO/OPTICAL INTERFACES NEXT TO THE CHIP WILL SIGNIFICANTLY IMPACT THE INDUSTRY. COULD YOU EXPLAIN HOW THE SUPPLY CHAIN WILL BE AFFECTED?

TT: The industry is currently facing significant connectivity bottlenecks, and this is forcing the various players to explore new approaches. One trend we are seeing is the breaking up of SoC monolithic dies into chiplets. Incorporating electro-optical chiplets inside the package, right next to the SoC core die, is a continuation of this trend. This in-package approach will require changes in the supply chain.

In addition to packaging with chiplets, fiber attach and test methodologies need to evolve. We are also seeing strong progress and commitment from the foundries – namely GlobalFoundries, Intel, and most recently, TSMC – in supporting integrated electro/optical components. Lastly, choosing to keep the lasers external is one way we are able to alleviate these supply chain complexities.

Standardization will also play a key role in addressing supply chain challenges and scaling this technology. Both UCIe and CXL are looking to address interconnects over optical fiber and are exploring the formulation of optical I/O specifications. Further, the CW-WDM MSA is a critical industry initiative that is defining and promoting new standards and specifications for optical laser sources. There is a tremendous need to develop and nurture this full ecosystem because optical I/O is such a revolutionary technology impacting so many areas of the industry.

MV: HOW WILL OPTICAL I/O TECHNOLOGY AFFECT OTHER APPLICATIONS?

TT: That is a great question. We have talked a lot about HPC and AI/ML already, but we also expect to see its use grow in other areas that require the rapid transfer of data such as in the cloud and datacenter, telecommunications, aerospace and defense, autonomous driving, AR/VR and more. As optical I/O matures and becomes even more cost-effective, we see the potential for it to meet the growing bandwidth, power and latency requirements of a wide range of applications.
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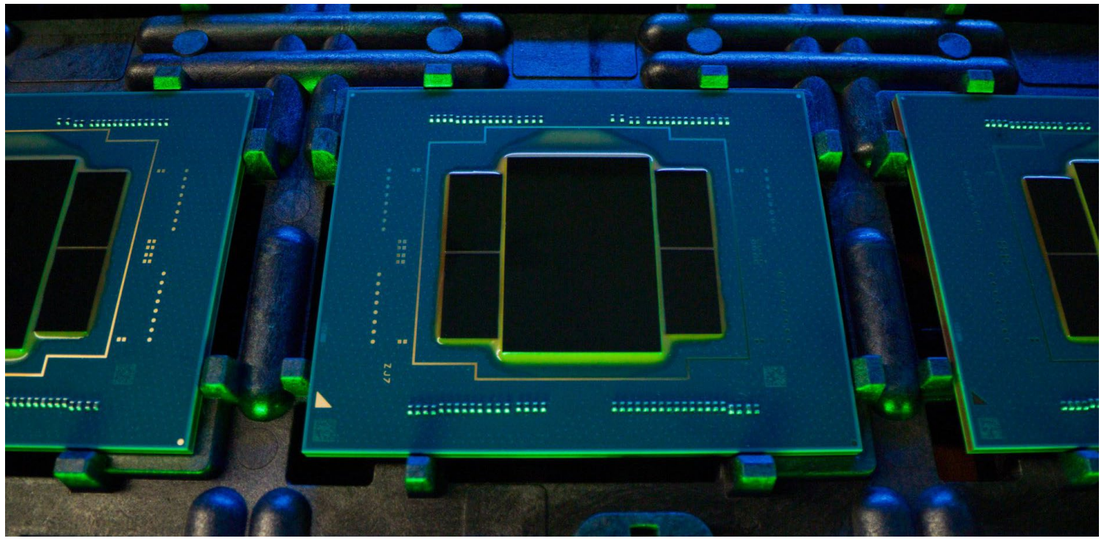

A multi-chip package with four Ayar Labs TeraPHY™ optical I/O chiplets and a customer's ASIC.

Courtesy of Ayar Labs, 2023

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QUADRIC

Transformers Broke Your NPU? Choose a General Purpose NPU Instead

by Steve Roddy, CMO at Quadric

Artificial Intelligence (AI) is the hottest of hot trends in the business of technology today. Machine learning (ML) – a subset of AI – is the focal point of that trend. ML is dramatically altering countless electronic systems in hundreds of end markets, and reshaping the underlying silicon technologies that power those systems. This trend began in earnest five or six years ago, and is only gaining momentum with each breakthrough in ML model creation. As result, a wide variety of System-on-Chip (SoC) designs across hundreds of end silicon markets are sold today in 2023 with some form of machine learning acceleration hardware included in the chip architecture.

Almost all of those designs today employ some form of Offload Engine or Accelerator – often labeled as an "NPU" or neural processing unit – paired with a legacy fully programmable processor. That legacy processor might be a CPU, a DSP, or a GPU but the concept is similar across all these designs: ask the software programmer to partition the machine learning (ML) workload to run the most performance intensive layers of the ML graph – typically the convolutions layers and activations - on the accelerator and allow the remainder of the inference to fallback to the programmable processor when and only if necessary to handle novel ML operators or complex code at the end of the inference process such as Softmax, ArgMax or NMS (non-maximal suppression).

Given the long design and production lead times for complex SoCs it is highly probable that the NPU in today's shipping silicon was designed by the chip architect in 2019 or 2020 to run the state of the art (SOTA) models of the day, such as the Resnet family of networks aimed at object detection for vision processing. The Resnet family (and similar networks) all featured very deep chains of convolution layers that form the "backbone" of the network. Predictably most NPU accelerators focused on convolution acceleration, thus most or substantially all of Resnet50 can run on the typical NPU accelerator. Problem solved. Or is it? Unfortunately for silicon architects, the SOTA in ML models changes far faster than the 24-36 month design and production cycles for silicon design. Today, the leading data scientist will want to deploy the current performance and accuracy standard bearers in the ML world – the Transformer. Vision Transformers (ViT) are the hottest new SOTA model that everyone wants to run and benchmark.

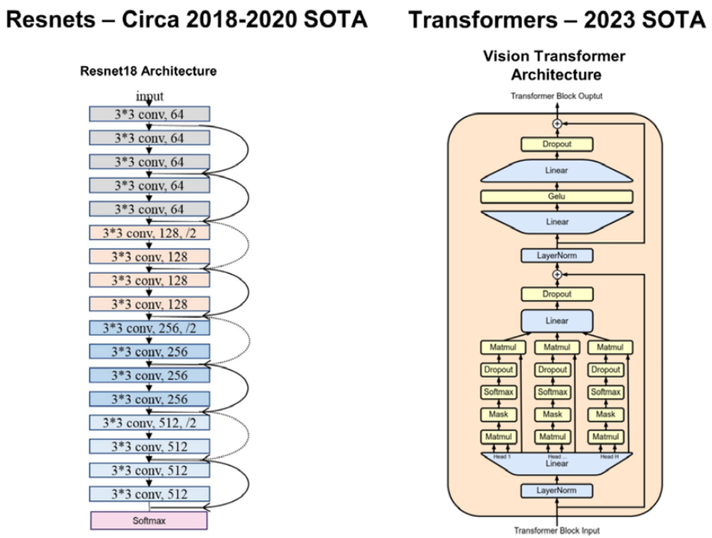

Figure 1 – A comparison of ML graph structure: Resnet vs ViT

Figure 1 shows the conceptual architectures of a Resnet family graph (left side) and an example of today's ViT architecture (right side). The reader doesn't need to be a data scientist or a processor designer to see that Resnet was a very straight-forward, iterative compute problem with very little variability and no complex control flow. Vision transformers are just the opposite. Resnet50 is comprised of only eight (8) ONNX graph operators, all but one (Softmax) is easily captured in an accelerator hardware machine. ViT by contrast employs twenty (20) graph operators - the bulk of which are non-matrix functions that cannot be mapped to the common accelerator architectures in today's silicon. The result: an accelerator optimized for Resnet likely cannot run Transformers at all. Thus today's silicon employing that hardwired accelerator may be completely unsuitable for future design-ins.

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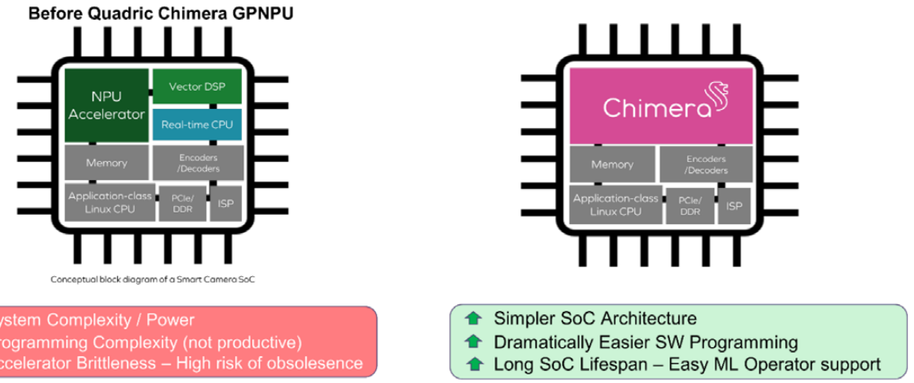


Figure 2 – A comparison of the traditional approach (left) and the Quadric approach

A BETTER APPROACH

Designers today need a flexible AI acceleration architecture to address the significant ML inference deployment challenges facing SoC developers. Quadric's ChimeraTM general purpose neural processor (GPNPU) is a simple yet powerful architecture with high matrix-computation performance and full C++ programmability. Its crucial differentiation is its ability to execute diverse workloads with great flexibility all on a single machine.

The Chimera GPNPU is a unified processor architecture that can handle matrix and vector operations and scalar (control) code in one execution pipeline. A Chimera GPNPU is entirely driven by code – both traditional DSP C++ code and ML graph code - empowering developers to continuously optimize the performance of their models and algorithms throughout the device's lifecycle.

THE BENEFITS OF USING A QUADRIC CHIMERA CORE ARE NUMEROUS:

System Simplicity

Quadric's solution enables hardware developers to instantiate a single core that can handle an entire ML workload plus the typical DSP pre-processing and post-processing signal conditioning workloads often intermixed with ML inference functions. Dealing with a single core drastically simplifies hardware integration and eases performance optimization.

Programming Simplicity

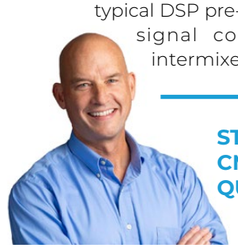
Quadric's Chimera architecture dramatically simplifies software development since matrix, vector, and control code can all be handled in a single code stream. ML graph code from the common training toolsets (Tensorflow, Pytorch, ONNX formats) is compiled by the Chimera software development toolkit (SDK) and can be merged with signal processing code written in C++, all compiled into a single code stream running on a single processor core.

Future Proof Flexibility – With High Performance

A Chimera GPNPU can run any algorithm written in C. Unlike competing IP solutions that tout "future proof" capability that runs new user code on a slow DSP or CPU, the Quadric solution runs user-written ML operators or custom C++ kernels at the same high-speed, highly-parallel performance levels as the "native" operators. Only a Chimera GPNPU delivers future-proof flexibility with high-performance.

As ML models continue to evolve and inferencing becomes prevalent in even more applications, the payoff from the Chimera architecture helps future proof chip design cycles. No one can predict which ML network will be state-of-the-art in 2026, but we can predict that Quadric's Chimera GPNPU will run that next breakthrough model at high efficiency.

www.quadric.io



STEVE RODDY
CMO,
QUADRIC INC

Steve Roddy is the CMO at Quadric Inc, the leading licensor of fully programmable general purpose neural processors (GPNPUs). Steve is a 27 year veteran of the semiconductor IP business with prior executive stints with Arm as VP Machine Learning Products, and Tensilica as VP Marketing and Business Development. He holds a Bachelors in EECS from UC Berkeley and an MBA from the Anderson School of Business at UCLA.

PORTFOLIO COMPANY ALUMNI
SPARK MICROSYSTEMS

Next Generation of Short-Range Data Transport

by Raphael Mehrbians, CMO, SPARK Microsystems

SPARK Microsystems is building next generation short-range wireless communication devices using its proprietary UWB technology. SPARK UWB, with its exceptional combination of high data-rate, low latency and low power consumption, enables new communication capabilities for next generation wireless mobile devices.

Unlike other companies offering UWB technology for positioning products like Apple's AirTag locators and keyless entry for vehicles, SPARK Microsystems is unique in exploiting ultra wideband technology for **short range data transport**.

The market opportunity that awaits SPARK UWB is significantly higher than positioning/location applications, and the implications for UWB in consumer and industrial markets are staggering. With SPARK UWB, the short-range wireless connectivity needs of tomorrow are being answered today for applications ranging from high-performance audio and gaming to AR, HIDs and IoT sensors – and beyond.

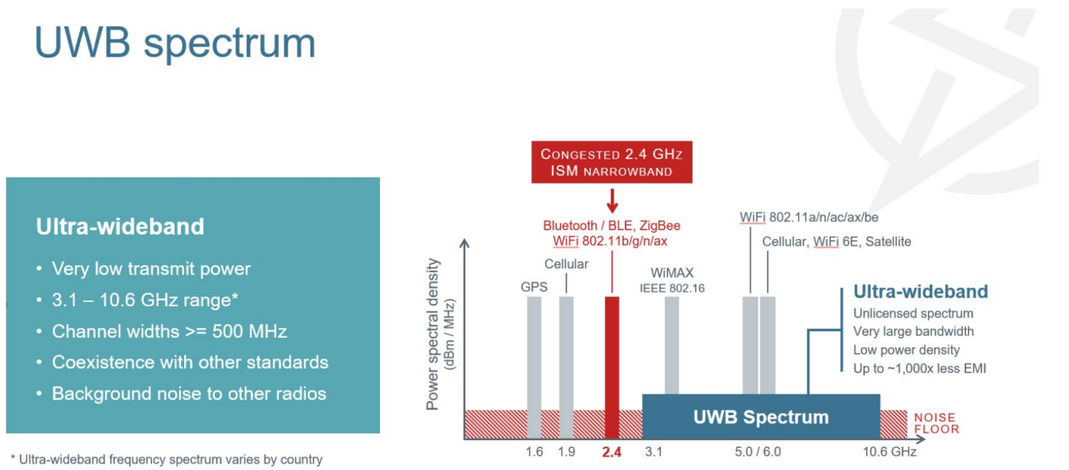
SPARK UWB delivers the performance advantages of wired connectivity – high data throughput and ultra-low latency – wirelessly for the first time.

And SPARK's UWB transceivers achieve the long-awaited holy grail for wireless connected devices: extremely low power consumption that ensures long uptime between device charging.

SPARK UWB complements legacy platforms like Bluetooth and Wi-Fi with a new high-performance, mobile-optimized connectivity layer. SPARK's technology enables wireless connectivity without compromise in performance or power efficiency for short-range Personal Area Networks. How does SPARK UWB achieve all this? It leverages ultra-low power impulse radio techniques across a wide, 3.1 to 10.6 GHz spectrum. Legacy platforms simply can't approach this performance because they are built on modulated carrier architectures and confined to congested narrow band spectrum.

The performance gains that SPARK delivers aren't just incremental. They are orders of magnitude better. SPARK UWB delivers 60 times lower power than Bluetooth, and 10 times lower power than Wi-Fi. It delivers 60 times lower latency than Bluetooth, with 20 times higher data rates. And it delivers 100 times lower power time-of-flight positioning than conventional UWB.

SPARK's breakthrough in this realm of PAN connectivity is essential for the coming era of consumer AR/VR devices, including smart glasses and other wearables. SPARK



SILICON STARTUP SOLUTIONS

RAPHAEL MEHRBIANS
CMO,
SPARK MICROSYSTEMS

Raphael Mehrbians joined SPARK in January 2022 as Chief Marketing Officer. Raphael has over 30 years of executive, marketing and business management experience spanning early-stage startups to publicly traded companies. Most recently Raphael was VP/GM at Adesto Technologies (acquired by Dialog Semiconductor/Renesas in 2020). He has held senior executive, business leadership and technical roles at Genesis Microchip, Lexar Media, Cirrus Logic and National Semiconductor in addition to executive management consulting roles at a variety of well-known semiconductor companies. Raphael has M.S. & B.S. degrees in Electrical Engineering from University of Michigan, Ann Arbor.

UWB delivers the unique ability to transmit huge volumes of data between devices with imperceptible latency, and real-time synchronization of audio, video and positioning data. And SPARK UWB does all this while consuming a fraction of the power of legacy short-range solutions.

Today, SPARK is working with our customers on consumer applications that finally – once and for all – can evolve beyond wired connectivity. This includes applications like high-performance audio, with SPARK UWB delivering CD quality, uncompressed stereo audio without wires. And it includes gaming peripherals like mice, headsets and keyboards capable of delivering wired-like performance with wireless freedom of motion – for the first time ever.

And this is just the consumer opportunity for SPARK UWB.

The opportunity in industrial IoT sensors is even larger, with implications for billions of connected devices in the coming decades.

SPARK's UWB technology holds the promise for a future of IoT sensors deployed without batteries or wires. Ultra power-efficient technology like SPARK UWB sets the stage for a future of battery-free IoT sensors that use energy-harvesting technologies to derive their own power.

The aggregate energy savings and reduced battery usage and replacements will ultimately help reduce landfill waste, CO2 emissions and other toxic environmental contamination. SPARK is deeply committed to solving challenges in environmental sustainability, and UWB represents a major step forward for cleaner tech.

For more information about SPARK Microsystems follow us at:
https://www.linkedin.com/company/sparkmicrosystems/
https://www.sparkmicro.com

PORTFOLIO COMPANY ALUMNI
MMTRON

mmTron
Unleashing the mmWave Frontier

Creating State-of-the-Art mmWave Power Amplifiers for Efficient, Reliable Performance

Multi-domain simulation with thermal analysis enables concurrent optimization of die, package, and PCB layout

mmTron, a Silicon Catalyst portfolio company based in Redwood City, California, specializes in designing high power, high linearity, yet efficient and reliable millimeter wave (mmWave) integrated circuits for advanced wireless and satellite communication systems. mmTron creates RF components in high-speed III-V processes, including GaAs, GaN, InP, SiGe, and RFSOI.

Dr. Seyed Tabatabaei founded mmTron in 2020 from his experience in RF test and measurement equipment circuit designs at Hewlett Packard, the birthplace of Keysight technology, and more recently, time at two other mmWave component design startups. mmTron's seven engineers use Keysight PathWave Advanced Design System (ADS) in a workflow with tools from Altium, Ansys, Cadence, and others.

The TMC211 is mmTron's latest 27-31 GHz power amplifier (PA). Its single-die GaN design delivers 50W power with 28% power-added efficiency (PAE), strong linearity, and a lowered operating junction temperature, which contributes to a higher mean time between failures (MTBF). Multi-domain electromagnetic (EM) and electro-thermal simulation capability in ADS and PathWave RFPro drives similar outcomes across mmTron's products.

CHALLENGE: DELIVER MORE POWER WITHOUT COMPROMISES

Much of the history of engineering has been a collection of practical tradeoffs during a project. Designers choose a set of parameters critical to their application and incorporate those in a design using physically implementable components and techniques to the best of their abilities. Attention then turns to sub-optimizing, maximizing a few desirable parameters while keeping others within acceptable limits. Classical hand calculations or single-domain simulation perform sub-optimization well.

Most manufacturers optimize RF PAs for the obvious parameter: maximizing the power a PA can deliver, with a secondary emphasis on linear performance across the operating bandwidth. More output power means more input power from the DC supply. Adding in power losses due to inefficiency and dissipated power in the PA translates to elevated junction temperature, lower reliability, and a shortened lifespan.

With more power amplifiers heading into long life cycle wireless communication applications – like defense and SATCOM – manufacturers have turned to multi-die PA solutions to spread power density across the package. Interconnect losses between dies cut power efficiency, linearity can be harder to control, and mmWave frequencies make effects more pronounced. Package size can also be a concern in aggressive SWaP-C (size, weight, power, and cost) environments.

Tabatabaei, shown in the lab in **Figure 1**, and his engineers asked: what would mmTron need to do to deliver more power with a single-die PA while still achieving linearity and SATCOM levels of reliability?

III-V processes like GaN provide the power density customers want. Arriving at a fully optimized design, unlocking the power potential while maintaining excellent linearity on a single die at a lower operating temperature, would require much more sophisticated behavioral models and simulation to account for cross-domain effects. "We knew going into the TMC211 design that thick metalization and close coupling between PA stages would create resonances making accurate EM simulation difficult," says Tabatabaei. A coordinated electro-thermal simulation would also be crucial for optimizing the design.

SOLUTION: AUTHENTIC WAVEFORMS AND ENHANCED MODELS IN MULTI-DOMAIN SIMULATIONS

Pushing the performance of RF components and system design calls for a suite of EDA tools for various tasks. Tabatabaei was deeply familiar with ADS, but some of mmTron's engineers were less familiar with the Keysight RF EDA environment. mmTron adopted Keysight PathWave ADS as the linchpin of its workflow, and its teams now see the advantages. "ADS enormously speeds up our product development because we can copy templates and set-ups quickly and start a new design," says Tabatabaei.

Templates are essential, but many EDA vendors offer templates. Another reason brought Tabatabaei to select ADS. "I definitely place a high value on Keysight's people," Tabatabaei continues. "The knowledge and skills they bring around ADS help us catch more issues earlier and work through situations like scripting, integration, and more that are extremely valuable in our mmWave RF component design efforts."

The next big decision for mmTron was a commitment to using authentic waveforms in ADS simulations. The alternative uses sinusoidal stimulation at several points across the bandwidth, then designing in excess margin, but the outcome is far less certain to predict as conditions change. "There are many PA subtleties that only appear under modulated signals," states Tabatabaei. "How the signal phase changes between stages, memory effects, interactions with capacitor values and placements, and power consumption all depend on modulation."

Optimizing high-frequency RF power amplifiers

ORGANIZATION
- mmTron

CHALLENGES
- High-power RF amplifiers commonly use multiple dies, giving up efficiency and size
- mmWave frequencies worsen losses and linearity
- Reducing die size increases thermal density and junction temperature, lowering reliability and service life
- Advanced III-V aging models are still scarce

SOLUTIONS
- Simulations with authentic waveforms, not sinusoidal frequency points, for modulated signals using PathWave ADS and PathWave RFPro
- Enhanced models in PathWave Device Modeling (IC-CAP) derived from GaN PDKs include thermal behavior, aging, and other features
- High-accuracy electromagnetic and electro-thermal simulation on a 48-core server

RESULTS
- TMC211 single-die layout reduces area by 60% while efficiently delivering 50W of power
- Lower die temperatures enable 15-year life targets
- 97% first-pass design success across mmTron

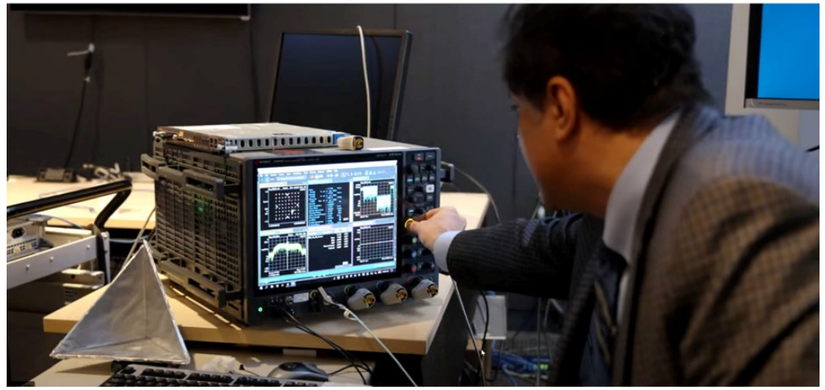


Figure 1 – mmTron founder Dr. Sayed Tabatabaei running tests in a lab

mmTron RF EDA tool stack

Workflow Step	EDA Tools
RF Device Modeling	**Keysight PathWave Device Modeling (IC-CAP)**
RF Circuit Design and Simulation	**Keysight PathWave ADS**
RF System Modeling and Simulation	**Keysight PathWave System Design**
3D Electromagnetic Simulation	ANSYS® HFSS™, Dassault Systèmes CST Studio Suite®, **Keysight PathWave RFPro**
Electro-Thermal Simulation	**Keysight PathWave ADS Electro-Thermal Simulator**
PCB Design and Layout	Altium Designer®, Cadence Allegro®

PORTFOLIO COMPANY ALUMNI
MMTRON CONT.

mmTron
Unleashing the mmWave Frontier

Customers are approaching mmTron with questions such as how crest factor and peak-to-average power ratio (PAPR) look in specific modulation scenarios. “Our core competence is using design and layout steps for optimizing the PA structure to provide the best performance in a modulated environment, and we have a lot of scripts written to help do that,” says Tabatabaei. For example, Keysight assisted mmTron in developing ADS scripts to help keep PA power delivery constant as modulation varies.

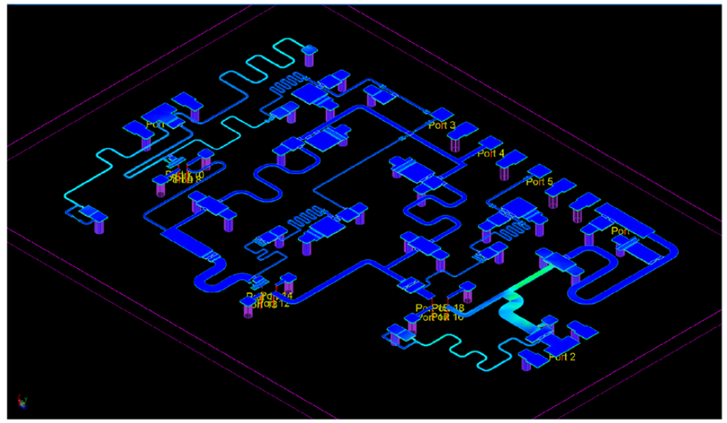


Figure 2 – Rendering of a mmTron power amplifier ready for EM and thermal simulation in Keysight PathWave ADS

Figure 2 is an example of the mmWave die structures mmTron creates using ADS, showing the thick metalization between some of the circuit elements.

Accurate simulation results and, ultimately, the quality of MTBF predictions also depend strongly on the robustness of behavioral models. Most commercially available process design kits (PDKs) for the GaN technology used in the TMC211 concentrate on functional performance, not aging. “We need to simulate drift, gate leakage, and more aging detail to predict MTBF accurately,” shares Tabatabaei. “We obtained DARPA-funded GaN models from a university and made substantial customizations reflecting the SATCOM environment, including different specifications for low-earth orbit (LEO) or geostationary orbits (GEO).”

Thermal modeling works hand-in-hand with EM modeling for coordinated simulation in ADS using the native EM simulator and the electro-thermal extension in a single, easy-to-use interface without layout conversions. Layout loops between a die, its package, and the printed circuit board (PCB) can pose issues. mmTron used ADS’s extensive stability analysis capability to optimize the die and package design together, along with a recommended PCB layout.

Load-pull analysis is a good example where advanced multi-domain simulation enhances accuracy. mmTron drew on years of experience with many ADS templates and some insight from Keysight customer success engineers in creating their custom solutions.

“We’re in a high-touch environment where we work closely with our customers,” says Tabatabaei. Often this extends beyond developing and running simulation scenarios on mmTron’s 48-core EDA server to performing corroborative measurements describing set-ups and test and measurement equipment for verification. mmTron can share ADS files or encrypted PDKs with mmTron enhancements for customers to run their own simulations. Whether customers can use a standard product once seeing how it simulates in their context or whether they need a specially designed derivative to meet requirements, mmTron can meet the need.

> “I definitely place a high value on Keysight’s people. The knowledge and skills they bring around PathWave ADS help us catch more issues earlier and work through situations like scripting, integration, and more that are extremely valuable in our mmWave RF component design efforts.”
>
> Dr. Sayed Tabatabaei, **Founder and CEO, mmTron**

Electrical Performance : Vdd = 28 V, Vgg = -3.7 V, TA = 25 °C, F = 29 GHz				
	min	Typ	Max	Units
Frequency	27		31	GHz
Gain		17		dB
Return Loss		10		dB
Psat		47		dBm
PAE		28		%
Bias Voltage		28		V
Bias Current		1700		mA

RESULTS: CREATING STATE-OF-THE-ART PAS FASTER

mmTron captures the benefits of using PathWave ADS innovatively in three areas. The first is creating the state-of-the-art TMC211 with what Tabatabaei describes as “unheard-of performance,” citing one key specification: 23W of linear power at a noise power ratio (NPR) of 19. Figure 3 shows a screenshot from the TMC211 preliminary datasheet (subject to change). According to Tabatabaei, Its single die is 60% smaller than competing multi-die amplifiers delivering less power.

Another benefit is a hybrid business model for mmTron. Tabatabaei says his teams have been able to turn derivative product designs for specific customer requirements in less than a month. mmTron is experiencing a growth spurt with four times the number of customer engagements during the first quarter of 2023 compared to prior years. Some of these customized designs may be spun back out as standard products if there is demand. The TMC211 began its journey as a derivation from a prior 25-29 GHz design, the TMC2111, done for a specific program before being standardized as an off-the-shelf product.

Finally are the internal metrics. Tabatabaei shares that his teams have a 97% first-pass success rate across all standard or custom product designs executed in ADS since mmTron’s inception. This success rate gives customers a high confidence level in mmTron, allowing mmTron to engage in more projects and scale their engineering resources effectively. “We’re able to plan our standard product roadmap two years out while still keeping the flexibility to grab customization opportunities where they make sense,” says Tabatabaei. He adds his team is branching out from PAs and RF front-ends to low-phase-noise oscillators and extremely broadband mixers with similar optimized performance and life cycles.

mmTron is also exploring the emerging sub-THz frequency space with customers, preparing for when process technology, test and measurement equipment, and viable economic volumes align.

LOOKING AHEAD: A SINGLE DESIGN COCKPIT

Tabatabaei suggests Keysight RF EDA tools cover the right design and simulation areas and exchange data cleanly. However, it would be even better if they all came together in a single design “cockpit.” For example, ADS and PathWave System Design currently launch as separate applications. “Shouldn’t PathWave System Design launch directly from the ADS user interface,” he muses. Transistor counts are rising as RF component complexity grows. mmTron has leveraged an affordable layout versus schematic (LVS) checking tool combined with extensive scripting in ADS, and better integration would help.

Learn more about mmTron and its mmWave RF signal chain products at:
www.mmTron.com
For more information on these Keysight RF EDA solutions, please visit:
PathWave Advanced Design System (ADS)
PathWave RFPro
PathWave ADS Electro-Thermal Simulator
Keysight EDA Software: First by Design

All figures courtesy of mmTron, Inc.

UNIVERSITY NEWS
BANATAO INSTITUTE

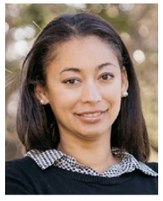
CITRIS and the Banatao Institute

Silicon Catalyst, the leading incubator for semiconductor startups, has joined forces with CITRIS (The Center for Information Technology Research in the Interest of Society) in an exciting collaboration that brings together student interns with the most innovative minds in the industry.

The goal is to bridge the gap between academia and the dynamic world of technology. With this partnership, University of California student interns now have a unique opportunity to dive into the center of innovation by connecting directly with Silicon Catalyst's impressive portfolio companies. This unprecedented access to cutting-edge projects and industry experts promises an immersive learning experience that goes far beyond the confines of a classroom. The stage is set for a remarkable exchange of ideas, forging the path for the next generation of semiconductor pioneers.

JILL FINLAYSON, MANAGING DIRECTOR, CITRIS INNOVATION HUB

"CITRIS is pleased to have SiCatalyst host students in the Workforce Innovation Program. Participating interns look forward to increasing their understanding of the semiconductor sector and the due diligence required for investing in startups." - Jill Finlayson, Managing Director, CITRIS Innovation Hub



NICOLE COTTON
PROGRAM MANAGER
CITRIS AND THE BANATAO INSTITUTE

"We are delighted to have SICatalyst join as a host in the CITRIS Workforce Innovation program. It is a timely addition our programs since we are expanding the semiconductor tract"

The CITRIS Workforce Innovation Program offers select University of California students the opportunity to inform their career decisions through eight-week paid internships, in which they'll build in-demand skills through on-the-job experience. Participants will receive training in leadership and project management, and will be supported throughout the internship program by dedicated CITRIS staff, as well as the community of peers in their cohort. Participating undergraduates represent a variety of majors at the four CITRIS campuses: UC Berkeley, UC Davis, UC Merced and UC Santa Cruz. Students are placed in one of five areas of emerging IT innovation important to the state of California: aviation, climate and energy, digital health, robotics, and semiconductors.

Special Thanks to Nicole Cotton who has been instrumental in helping match the UC students with our portfolio companies. Silicon Catalyst will host two interns from the CITRIS Program, our Portfolio Company Siloxit will host three.

NAIA DALAL
SILICON CATALYST INTERN

My name is Naia Dalal and I am an electrical engineering student at UC Davis. With a strong interest in entrepreneurship, I plan to minor in Technology Management to complement my technical skills. In my free time, I enjoy solving puzzles, rollerblading, and working on DIY projects. I am excited about the opportunity to learn new skills and collaborate with professionals in my upcoming internship with Silicon Catalyst.

SEAMUS KELLY
SILICON CATALYST INTERN

My name is Seamus Kelly, a junior at UC Santa Cruz, pursuing a major in electrical engineering with a concentration in optics and electronics. I have found a passion for the complexities of FPGA/ high speed digital design; I love the challenge that comes from trying to implement complex systems that push the boundaries of what I am currently capable of and furthering my understanding and experience in electrical engineering. I am driven to discover and further my understanding of electrical circuits and electrical systems in the world around us to better myself as an engineer and leave behind a legacy of advancements in technology and betterment of the world around us.

Industry Partners

NEXTCORPS LUMINATE

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MITRE ENGENUITY. A Foundation for Public Good

ASIC American Semiconductor Innovation Coalition

PRAXIS CENTER for Venture Development

SEMICONDUCTOR REVIEW
PHOTONICS

Silicon Catalyst: An Accelerator Created Just for Semiconductor Startups

www.semiconductorreview.com

Semiconductor companies have seen drastic growth in the number of patents, market share, and revenue. Despite these impressive numbers, raising funds in the semiconductor industry is not as easy as it might seem. See the graph on page 64 from the CHIPS Act report, www.chips.gov citing the percent of venture capital investment in semiconductors since 2001.

DAN ARMBRUST
CO-FOUNDER, DIRECTOR

PETE RODRIGUEZ
CEO

Numerous investors and analysts believe that the sector is suffering from a funding "moat" issue, which prevents capital from flowing in due to a lack of transparency and risk associated with semiconductors. More than funds, however, these companies need support and direction in their early years, which has been the mission of Silicon Catalyst since launching in 2015.

Hailing from Silicon Valley and with Partners based in Israel and England, Silicon Catalyst is the only incubator in the world that is focused on startups in the semiconductor industry. It provides access to funding, mentorship, and industry expertise to startups that create innovative technologies including Photonics, IP, MEMS, Sensors, and Life Sciences.

To date, Silicon Catalyst has screened over 800 startups and created a portfolio of companies worth more than $1.5 billion. Silicon Catalyst also boasts an extensive network of 300+ investors and advisors who are semiconductor veterans with deep experience in the industry.

"Our investors and advisors help startups carve a path to success by providing guidance on business planning market fit, understanding the customer environment and building a winning team," says Pete Rodriguez, CEO of Silicon Catalyst. "Companies in our incubator receive millions of dollars of in-kind products and services, at no-cost or at a significantly reduced rate from their standard fees.

The annual listing of 10 companies that are at the forefront of providing Photonics solutions and transforming businesses.

This includes EDA licenses from Synopsys, IP from Arm and most importantly free MPW shuttle runs with TSMC. The net outcome is an acceleration of their business growth while saving them several million dollars."

Silicon Catalyst is not just another accelerator. It takes a keen interest in every startup it selects for its incubation program. That is why the company considers itself a partner that helps entrepreneurs turn their dreams into reality. "We're extremely excited to have formed an alliance with Mayfield, the legendary venture capital firm for the semiconductor industry, as they will invest capital and provide mentoring to the majority of seed stage companies admitted to our incubator," stated Pete Rodriguez.

Other than investors and advisors, the firm has a thriving strategic partner ecosystem made up of big names in the semiconductor industry, including Arm, Bosch, NXP, Sony Semiconductor Solutions, ST, TI and collaborates with other incubators, including Luminate, focused on optics, photonics, and imaging. Silicon Catalyst also has an

> ***"Our investors and advisors help startups carve a path to success by providing guidance on planning market fit, understanding the customer environment and building a winning team"***

industry. The relationship panned out quite well for the startup, as it has now raised a seed round of $11.5 million to continue building high-speed multi-chip processors to accelerate exponential advances in AI.

Finding such innovative and capable companies is Silicon Catalyst's primary focus. That is why the firm has helped launch the Silicon Catalyst Angels investment group, which provides seed and Series A funding to semiconductor startups. It has over 50 accredited investors who conduct comprehensive due diligence to select and provide early-stage investments to help the startups get off the ground.

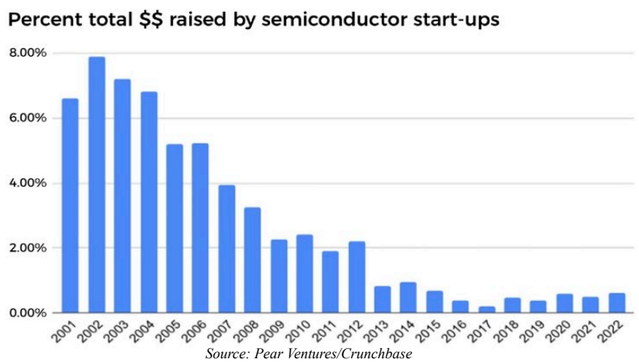
array of partners - called In-Kind Partners (IKPs) - that offer highly discounted goods and services for Silicon Catalyst to distribute to its startups that have joined their incubator.

To add perspective, MathWorks is one of the more than 60 Silicon Catalyst IKPs that allows companies in the incubator to use its products free of cost during the 24-month incubation period. With such a strong network of advisors and partners, Silicon Catalyst has incubated companies that are fueling the next generation of semiconductor innovations.

Salience Labs www.saliencelabs.ai is one such firm in the Silicon Catalyst 24-month program, that is building a hybrid photonic-electronic chip for AI. The startup is based on decades of research collaboration between Oxford University and the University of Münster, Germany. Silicon Catalyst has played a significant role in incubating the UK-based startup, giving it the much-needed exposure and resources to make its mark in the

Silicon Catalyst takes immense pride in its team of highly talented people that start from co-founder and former CEO, Dan Armbrust. He is one of the official members of the Industrial Advisory Committee of the Department of Commerce, as part of the CHIPS for America Act, that advises the White House on semiconductor innovation. It should be noted that Dan is a coauthor of a recently published 2-part article in the Georgetown Public Policy Review, "America's lead in advanced computing is almost gone."

The coming years for Silicon Catalyst will be exciting, to say the least. The firm has already expanded its footprint off shore, opening offices in the UK and Israel. It is also planning to increase its pool of incubation programs to 250 startups by 2025. However, one thing that will remain unchanged, is the passion and determination of Silicon Catalyst to find promising startups and help them become the next big thing in the semiconductor industry.



Source: Pear Ventures/Crunchbase

COMPANY
Silicon Catalyst
www.siliconcatalyst.com
HEADQUARTERS
Silicon Valley, England and Israel
MANAGEMENT
Dan Armbrust, Co-Founder and Director
Pete Rodriguez, CEO
DESCRIPTION
Silicon Catalyst is the world's only incubator focused on semiconductor solutions, including photonics, MEMS, sensors, IP, materials and life sciences.

SiliconCatalyst.UK
IMAGINATION TECHNOLOGIES

A big thank you to our Silicon Catalyst In-Kind Partner, Imagination Technologies, for hosting and partnering with us on Thursday March 30th for a unique UK based event

“Semiconductors Question Time”

We gathered approaching 100 UK Semiconductor executives in the splendid atrium of Imagination House, Kings Langley on the outskirts of London in the UK, to discuss and debate the importance of government semiconductor strategies around the world.

Sean Redmond, our UK Managing Partner for Silicon Catalyst, set the scene by asking the audience to imagine where the UK semiconductor design industry would be if the UK Government had not implemented its last semiconductor strategy in 1979. There would quite possibly have been no Inmos, which was supported by the UK government at that time. Inmos gave birth to one of the world’s first parallel processor architectures, the Transputer and a rich pool of processor design expertise. Inmos was subsequently acquired by SGS Thompson, which became ST. Hence with no Inmos, there would not have been a STMicroelectronics Bristol site. Some of our most successful fabless semiconductor startups were created by teams that cut their teeth in STMicroectronics. Element 14, Icera and subsequently Graphcore for example may never have been created. XMOS was also founded by an ex-Inmos genious, David May. Sir Hossein Yassaie was ex Inmos, so again there probably would have been no Imagination Technologies. Acorn’s transition to a chip design team, was fuelled by skills from Inmos, so without Inmos there may never have been an Arm.

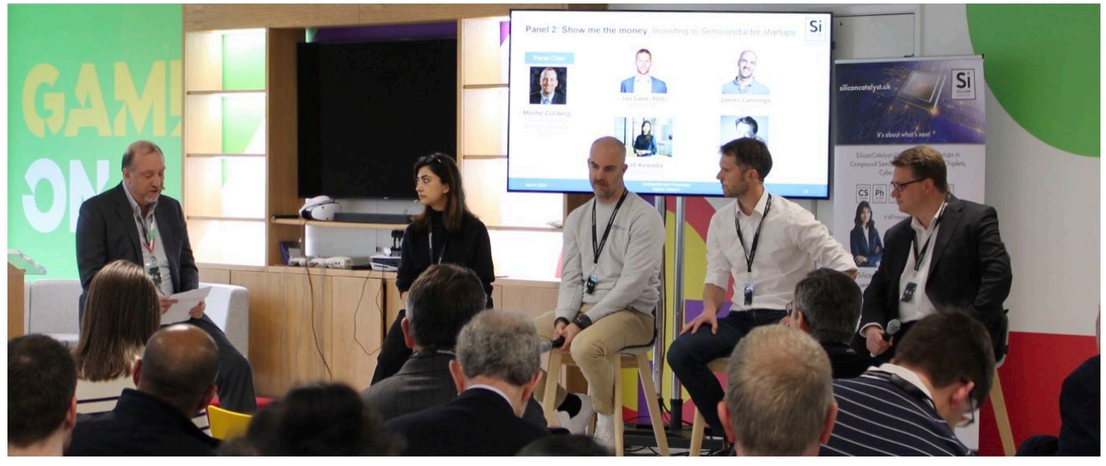
We started the evening with a very warm welcome from Ray Bingham, Executive Chair of Imagination. He provided great insight into the accelerated progress they are making, which the strong investment backing his team has delivered. This was followed by Jim Wallace, strategic business development director from Imagination Technologies, projecting the value of their open access semiconductor startup program.

The effervescent semiconductor industry analyst Malcolm Penn blew our ears off with a rollercoaster ride through his semiconductor industry four horse men of the apocalypse forecast analysis. It certainly doesn’t look like any one of the horses will save the day in ‘23.

Silicon Catalyst UK Ltd has been commissioned by the UK government Department for Science, Innovation & Technology (DSIT) to undertake a study into infrastructure

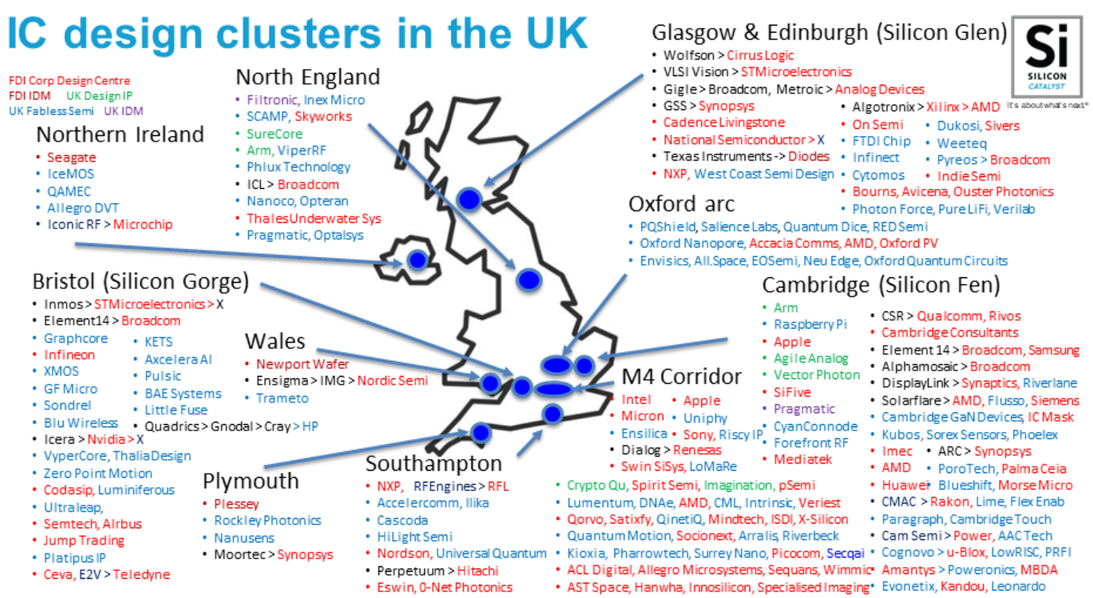
SILICON STARTUP SOLUTIONS

SiliconCatalyst.UK
IMAGINATION TECHNOLOGIES



to grow the UK semiconductor industry and a new strategic coordination function for the sector. Sean Redmond, our UK Managing Partner, shared with the audience the vibrance of the UK IC design company landscape by presenting a cluster map of 193 unique companies shown across the UK, many with multiple sites.

The event then launched into the first panel discussion of the afternoon, chaired by Sean Redmond, by challenging the panel with debating the biggest elephant in the room, government semiconductor policy interventions. Starting with a deep dive on the EU CHIPS Act from Malcolm followed by comparisons to the US CHIPS act from the extremely knowledgeable Dr John Goodenough. Then the wonderful Giorgia Longobardi, founder and CEO of Cambridge GaN Devices, projected out the opportunities for GaN semiconductor market growing at a staggering 57% CAGR to north of $2Bn by ‘27. Firmly planting the flag for the need for an open compound semiconductor fab in the UK. Our most successful UK semiconductor CEO, Jalal Bagherli, then stressed the importance of international collaboration with all government semiconductor policy interventions to make sure they all complement one another.



The second panel session of the afternoon was chaired by our gregarious Silicon Catalyst Managing Partner from Israel, Moshe Zalcberg. Russell Haggar, one of our UK based Silicon Catalyst advisors, talked about the near extinction event of Silicon Valley Bank. The brilliant Vaysh Kewada, CEO of our UK portfolio company Salience Labs, enthused about the help she received from Silicon Catalyst to help raise her very successful seed round. Followed by James Cannings, the CEO of one of newest UK portfolio Companies QPT, gave his insights into the very attractive tax benefits on offer in the UK from the Seed Enterprise Investment Scheme. Before opening the floor for questions, Ian Lane from one of the UK leading semiconductor VC's, Cambridge Innovation Capital, gave a very clear explanation of how startups can use convertible loan notes.

The event was capped off with very productive networking over a splendid buffet dinner and enthusiastic sampling of Castello Redmond '22 made organically in the UK from Montepulciano grapes imported from Abruzzia in Italy by our Managing Partner, Sean.

PORTFOLIO COMPANY
RAAAM

EnICS Labs in Bar Ilan University

RAAAM Memory Technologies, which develops a very efficient embedded memory, joined Silicon Catalyst last year. RAAAM's technology was jointly developed over several years by Bar Ilan University (BIU) in Israel and Ecole Polytechnique Federale de Lausanne (EPFL) in Switzerland.

This prompts us to turn a spotlight on BIU, and specifically the Emerging Nanoscaled Integrated Circuits & Systems (EnICS) Labs in its Faculty of Engineering, which were founded in 2015, have played and are continuing to play an important role in Israel's semiconductor innovation scene.

EnICS was initiated by Professor Alexander (Alex) Fish, who realized at the time that true innovation in semiconductor research and development required collaboration between various groups of faculty and researchers, as no single group could have the necessary resources by itself. To realize his vision, he recruited three other researchers – Professor Adam (Adi) Teman, Professor Yossie Shor, and Professor Osnat Keren, all of whom are still part of the EnICS leadership team. Alex and Adi are also co-founders of RAAAM, together with Robert Giterman (CEO) and Professor Andreas (Andy) Burg from EPFL.

In line with its vision, EnICS is all about collaboration.

In Israel, one of the flagship programs of the Israel Innovation Authority (IIA) is Magnet. Magnet are consortia, consisting of academia, industry (both large companies and start-ups), and occasionally other entities, that join forces to work on long-term R&D projects with potentially big impact. Participating companies get 66% of the approved Magnet budget and the academia gets 100% from the IIA, which also funds a consortium coordinator. Since its inception, EnICS has played a key role in two Magnet consortia. The first one was focused on shortening development time and increasing performance of SoCs, and the more recent one was dedicated to a RISC-V-based compute platform. In the latter, EnICS collaborated with companies such as DSP Group (later acquired by Synaptycs), Mellanox (later acquired by NVIDIA), CEVA, Dolphin Integration (later acquired by SOITEC), and Western Digital, as well as with the Technion, Tel Aviv University, and Ben Gurion University.

EnICS also has a broad range of collaborations with universities outside of Israel. In addition to EPFL, already mentioned above, it partners with universities in the US, Italy, Finland, Cyprus, Sweden, and more. These collaborations take a variety of forms, including BIU faculty and staff members spending time working at partnering universities and EnICS hosting faculty and staff from those universities.

EnICS also has very strong relations with TSMC. Since 2018, EnICS has been hosting an annual innovation event at the Faculty of Engineering as part of the TSMC Open Innovation Platform (OIP). Following the popularity and success of these events, TSMC has decided to expand the event this year into a large, multi-track OIP event.

Today EnICS has seven labs – analog, hardware security, digital measurement, image sensors, reliability, SoC, and a student design lab. In addition to its 6-person leadership team (Dr. Itamar Levy and Dr. Leonid Yavits joined the founding four), it has an engineering team of eight people as well as administrative support. Financially, EnICS is self-sufficient. It gets all its funding from research grants and projects it does for the industry, including to the defense sector.

As already mentioned, Silicon Catalyst portfolio company RAAAM was co-founded by Profs. Alex and Adi, along with Robert Giterman (CEO) and Professor Andreas (Andy) Burg from EPFL. The company's name RAAAM is actually the initials of the founding team, which is very convenient for a memory technology company...

We at Silicon Catalyst are looking forward to additional innovation coming out of BIU and EnICS.

SILICON CATALYST ANGELS

We are inviting potential investors to take a dive into a world where groundbreaking technologies are nurtured, innovations are ignited, and the future is transformed. The Silicon Catalyst Angels group is an investment offshoot of Silicon Catalyst, the singular incubator devoted solely to propelling advancements in semiconductor solutions.

What sets Silicon Catalyst Angels apart is not just our unparalleled access to an exclusive stream of cutting-edge opportunities, but the extraordinary composition of our membership - a league of seasoned semiconductor veterans, armed not only with their investment prowess but also with deep industry knowledge and expertise.

The angels' members possess a deep understanding of the hardware landscape, cultivated through decades of experience in the semiconductor industry. The true magic lies in the fusion of our members' unparalleled experience, and vast network of connections with the exceptional companies that have been meticulously vetted and welcomed into the Silicon Catalyst family.

After launching our group in July 2019, we're pleased to announce that our members have invested over $2.5 Million in 17 companies, 15 of which are from the Silicon Catalyst Incubator/Accelerator.

Interested in joining?
Interested in pitching?

Please contact Laura Swan
laura@siliconcatalystangels.com
siliconcatalystangels.com

Amos Ben Meir
Board President

Michael Joehren
Director

Raul Camposano
Director

Laura Swan
VP. Operations

AyarLabs
DOVER MICROSYSTEMS
EnCharge AI
ERIDAN
ESPRE TECHNOLOGIES
IMPRINT ENERGY
Lelantos
Lemurian Labs
MENTIUM TECHNOLOGIES
mmTron Unleashing the mmWave Frontier
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OWL AUTONOMOUS IMAGING
PHINOMICS
POLYN TECHNOLOGY
RAAAM The Highest Density On-Chip Memory in Standard CMOS
XCELERIUM
ZEPSOR TECHNOLOGIES

SILICON STARTUP SOLUTIONS

SILICON CATALYST ANGELS
ANGEL CAPITAL ASSOCIATION

Silicon Catalyst, Silicon Catalyst Angels (SCA) and The Angel Capital Association (ACA) are forging an alliance to create a semiconductor **investment coalition**. Their shared mission? To amplify capital investment in early-stage semiconductor startups.

The surge of interest in semiconductor deals has reached unprecedented heights, fueled by the CHIPS and Science Act of 2022. The pervasive presence of chips in our daily lives, from smartphones and laptops to cars, home appliances, and cutting-edge technologies like advanced driver assistance systems (ADAS) and electric vehicle components, presents an irresistible case for investing in the semiconductor domain.

The momentum behind semiconductor deals is galvanizing angel groups, compelling them to collaborate in syndicating deals. The allure is crystal clear: reduced financial risk, collective wisdom in due diligence, and an infusion of capital for a multitude of companies. The synergy among these entities is poised to reshape the landscape of semiconductor investments, heralding

ACA
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an exciting new era in technological innovation and financial opportunities.

In the dynamic realm of angel investing, the Angel Capital Association (ACA) emerges as a driving force, uniting their community of angel investment groups (~250), with over 16,000 accredited investors across the United States. The ACA is a powerful ally, empowering angel investors with a wealth of resources, support, and opportunities. The ACA equips its members with invaluable education, fostering a culture of continuous learning and growth. Through their extensive network, investors gain access to an expansive community igniting innovative ideas and partnerships. Moreover, the ACA advocates for the interests of angel investors, amplifying their collective voice on matters that shape the investment landscape.

By harnessing the collective expertise and capital of its members, the ACA breathes life into diversification, enabling investors to expand their portfolios and enhance their prospects of success. Together, they forge a robust front, bolstered by shared wisdom, pooled resources, and a shared commitment to fueling entrepreneurial endeavors.

With their fingertips on the pulse of innovation, Silicon Catalyst and SCA tap into the collective intelligence and in-depth industry experience of their vibrant semiconductor ecosystem of diverse perspectives and learnings. SCA's understanding of collaboration and synergy has led them to forge strong relationships with other investment groups like Sand Hill Angels, Band of Angels, and Tech Coast Angels. These powerful alliances have birthed a new era of deal syndication, amplifying the pool of early-stage angel investors drawn to SCA's vision.

The collaboration between Silicon Catalyst, ACA and SCA turbocharges industry growth, igniting a cascade of opportunities for early-stage angel investors to unite under a common mission to fuel semiconductor innovation in the U.S.

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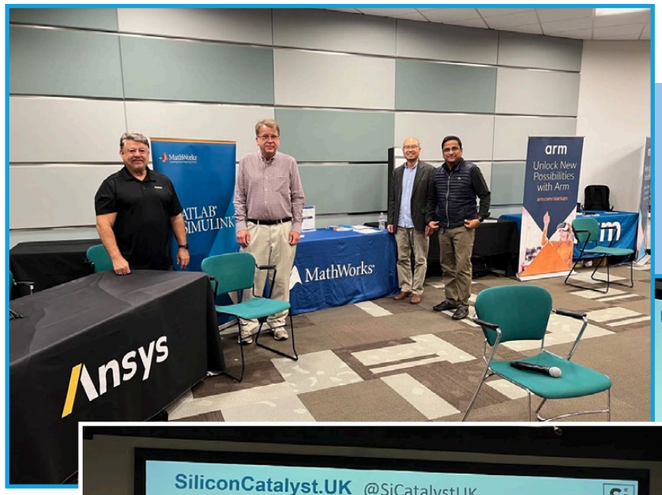

About Us

Silicon Catalyst is the world's only incubator + accelerator focused on semiconductor solutions, including Photonics, MEMS, sensors, IP, materials and Life Science. We accelerate startups from idea through prototype, and onto a path to volume production.

We have engaged with more than 900 semiconductor startups worldwide and have admitted 97 exciting companies.

Our companies participate in a 24-month customized incubation program. Each is guided closely by a Silicon Catalyst partner. This includes a semiconductor focused curriculum and over 45 events worldwide each year.

Silicon Catalyst's ecosystem provides everything our startups need to design, fabricate, and market semiconductor solutions:

• **In-Kind Partners** (TSMC, Synopsys, Arm, ST, MathWorks and over 50 more) – provide each startup several millions of dollars' worth of goods and services including EDA tools, IP, PDKs, prototypes, design and test services, packaging and business solutions.

· **Strategic Partners** (including TI, Soitec, Bosch, Cirrus Logic, Arm, ST, Sony, EMD Electronics and NXP) – participate in the selection process and actively look for opportunities to partner with our startups.

· **Investors** – Our partnership with Mayfield and a large group of over 300 VCs, Angels, Angel groups, Corporate VCs, and Family Offices fund each journey. Silicon Catalyst Angels, created from our ecosystem, also funds our companies.

· **Advisors** – A valuable network of over 250 industry experts that we match to the specific needs of each startup.

· **Universities, Industry Organizations, Incubators, and Government Agencies** – We nurture dozens of key relationships for the benefit of our portfolio companies. Our companies have received over $100M in grants.

Silicon Catalyst's mission is to help semiconductor startups succeed. Join us in driving innovation!

Silicon Catalyst Angels was formed to foster the startup companies admitted into the Silicon Catalyst incubator. Comprised of seasoned semiconductor veterans who bring with them a wealth of knowledge along with their ability to invest, they are driven by passion and a desire to 'give back'. Our members understand the hardware space thanks to a lifetime of engagement in the industry. When you couple our members' enthusiasm, knowledge, and broad network of connections with companies that have been vetted and admitted to Silicon Catalyst, you have a formula that is to date, non existent within the investment community.

A VALUABLE RESOURCE FOR THE SEMICONDUCTOR STARTUP COMMUNITY

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