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Silicon Catalyst Portfolio Company Spring 2020 Update

06.16.20
06.18.20

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Portfolio Companies

CURRENT

Teramics
Leading mmwave Solutions

MultiFractal SEMICONDUCTORS

5D SENSING

MEMTECH

DiGiTAL Light

SigmaSense

beam

OWL
AUTONOMOUS IMAGING

DOVER MICROSYSTEMS

quadric

trameto

SPARK MICROSYSTEMS

ERIDAN

MENTIUM TECHNOLOGIES

Zeno SEMICONDUCTOR

ESPRE TECHNOLOGIES

Seamless Microsystems
Digitizing Your World Seamlessly

Power Down Semiconductor

June 16, 2020

Welcome to Silicon Catalyst's Spring 2020 Portfolio Company Update. We truly appreciate your participation and hope you and your families are staying safe.

This meeting is being held as an on-line event, as we believe it's most appropriate due to the challenges that we're all facing due to the pandemic.

We would like to thank all of our Ecosystem partners and especially to Arm and STMicroelectronics. Each of these companies have joined our ecosystem as both Strategic and In-Kind Partners.

arm

life.augmented

Some highlights since the Fall Portfolio Company Update in November 2019 held at TSMC:

- We held our 11th screening event and our first online in April and we had nearly twice the number of participants of our regular in-person attendance

- We now welcome 4 new companies into our family of Portfolio Companies:
5D Sensing, California Memory, Multifractal and Teramics bringing our total to 30 companies that have been admitted to our Incubator

- Mentor, a Siemens company, has joined as a new In-Kind Partner

- Silicon Catalyst Angels, launched in July 2019, will end their first year of operation with funding for 5 companies from our Incubator

- Our Joint Venture with Silicon Power Technologies in Chengdu China was launched in January 2019 and has already admitted 12 portfolio companies

- Continued expansion of our Advisor ecosystem, now in excess of 170 members

- Our network of Investors which includes VCs, corporate, angels and angel groups, now in excess of 250.

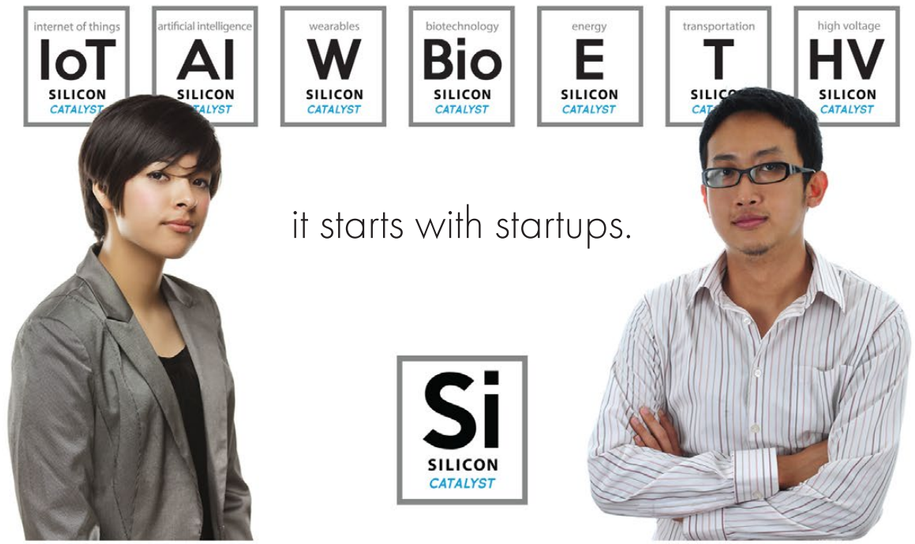
- Launched our university and accelerator program, with events held with semiconductor industry major centers of learning

Thank you for your continued support of our efforts to build a world-class ecosystem for startup companies focused on accelerating solutions in silicon.

Pete Rodriguez
CEO

Startups start here.

it's about what's next.®



APPLICATIONS NOW BEING ACCEPTED

Deadline: July 6th

Our global outreach is underway to find early-stage semiconductor startups to join our incubator

Silicon Catalyst is the world's only incubator focused exclusively on accelerating solutions in silicon, building a coalition of in-kind and strategic partners to dramatically reduce the cost and complexity of development. More than 300 startup companies have engaged with Silicon Catalyst since April 2015, with a total of 31 startup and early-stage companies admitted to the incubator developing innovative solutions in a variety of areas including energy harvesting, wearables, silicon photonics, memory technology, IoT, high performance computing, artificial intelligence, machine learning, wireless communications, and biomedical devices.

The Silicon Catalyst incubator utilizes our coalition of in-kind and strategic partners to dramatically reduce the cost and complexity of developing semiconductor solutions. With our world-class network of mentors to advise startups, we are addressing their many challenges in moving from idea to realization and business success. We have provided our Portfolio Companies with a path to funding, free access to tools, testing and shuttle runs, along with advice on proper corporate governance and strategic execution.

Contact: Richard Curtin, Managing Partner
richard@sicatalyst.com

www.siliconcatalyst.com

About Us

Silicon Catalyst is the world's only incubator focused exclusively on accelerating solutions in silicon. We address the challenges faced by these startups while guiding them from idea to prototype, and then to product. Over 300 startup companies have engaged with Silicon Catalyst since April 2015, and we have admitted 30 exciting companies.

Silicon Catalyst exists to help semiconductor startups succeed. We have created a growing ecosystem of In-Kind partners, industry-leading companies, expert advisors, investors, leading universities and industry organizations such as the Global Semiconductor Alliance and SEMI, which enables our startups to form deep relationships with people that provide value to their long-term success.

We provide the startups we incubate with several millions of dollars worth of goods and services from our network of industry-leading In-Kind partners to dramatically reduce the cost of development. These goods and services include EDA tools, PDK access, foundry wafers, test equipment, design services, and other valuable technical and business capabilities which include, but are not limited to, software development, patent filing, and financial management.

Silicon Catalyst startups interact with a valuable network of expert advisors. In addition, our strategic partners share their experience and actively look for opportunities to work together with our startups.

Our two-year incubation program also provides a path to funding through our connections with venture capitalists, strategic investors, individual angel investors, angel investment groups, and government agencies that provide grants.

In our first year we were awarded the prestigious UBM Canon Startup Company of the Year, in anticipation of our impact on the semiconductor industry. We are proud to have created a broad ecosystem which provides our startups with the greatest opportunity for a successful exit.

Silicon Catalyst Angels was formed to foster the startup companies admitted into the Silicon Catalyst incubator. Comprised of seasoned semiconductor veterans who bring with them a wealth of knowledge along with their ability to invest they are driven by passion and a desire to 'give back'. Our members understand the hardware space thanks to a lifetime of engagement in the industry. When you couple our members enthusiasm, knowledge, and broad network of connections with companies that have been vetted and admitted to Silicon Catalyst, you have a formula that is to date, non existent within the investment community.

A VALUABLE RESOURCE FOR THE SEMICONDUCTOR STARTUP COMMUNITY

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Spring 2020 Portfolio Company Update Agenda

June 16, 2020 - Portfolio Update Day 1
Webinar

Time	Company	Presenter
10:00 - 10:10	Silicon Catalyst Kick Off	Pete Rodriguez, CEO Tarun Verma, Managing Partner
10:10 - 10:20	Probius Dx	Emmanuel Quevy, CEO
10:20 - 10:35	Trameto	Huw Davies, CEO
10:35 - 10:45	Arm	Will Abbey, SVP
10:45 - 11:00	Quadric.io	Veerbhan Kheterpal, CEO
11:00 - 11:15	SigmaSense	Rick Seger, CEO
11:15 - 11:25	ST	Kirk Ouellette, VP Corporate Strategy
11:25 - 11:40	Mentium Technologies	Mirko Prezioso, CEO
11:40 - 12:55	Dover Microsystems	Jothy Rosenberg, CEO
11:55 - 12:00	Wrap Up	Tarun Verma, Managing Partner

June 18, 2020 - Portfolio Update Day 2
Webinar

10:00 - 10:10	Silicon Catalyst Kick Off	Pete Rodriguez, CEO Tarun Verma, Managing Partner
10:10 - 10:25	Owl Autonomous Imaging	Chuck Gershman, CEO
10:25 - 10:40	Zeno Semiconductor	Yuniarto Widjaja, CEO
10:40 - 10:50	Arm	Will Abbey, SVP
10:50 - 11:-5	Beam Semiconductor	Stacy Joseph, CEO
11:05 - 11:20	Eridan Communications	Doug Kirkpatrick, CEO
11:20 - 11:30	ST	Kirk Ouellette, VP Corporate Strategy
11:30 - 11:45	Espre Technologies	John Terry, CEO
11:45 - 12:00	Spark Microsystems	Fares Mubarak, CEO
12:00 - 12:05	Wrap Up	Tarun Verma, Managing Partner

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5D SENSING

5DSENSING

Advanced CMOS sensors for Smart and Safe City

Problem

The huge cost of safe-city installation is due to communication infrastructure and datacenter costs. By pushing the detection and processing capabilities to smart cameras at the edges of the network, we can achieve a major reduction of infrastructure needs. Therefore, advanced sensors are the key technology to allow smart cameras, hence a key enabler for the safe-city market.

Solution

5D SENSING built a unique sensor that solves the "smart camera" sensing technology requirements by adding the 2D night vision, 2D daylight vision, ULL and 3D point cloud into a single CMOS sensor. All those data readouts of 2D and 3D concurrently with same field of view allows the image processing in the camera to yield better performance.

5D SENSING is using multiple technologies to make those advanced sensors: proprietary AMS readout circuit for the SPAD detector, proprietary time domain signal processing allowing getting both 2D and 3D images concurrently, advanced noise cancellation to implement S-SiPM, wafer bonding, back-side illumination and optical optimizations.

Technology

5D SENSING technology is focused on the readout circuits for SPAD arrays. The readout of the SPAD is converted into digital time-domain signal. The time domain signals are processed on pixel level local domain adding position data to the signal.

With time domain and spatial resolution data, each SPAD fire is translated into depth and intensity. Moreover, on local domain, multi-SPAD are averages to preform D-SiPM action of noise reduction. The local calculation improves resolution, SNR and allows to get night vision ultra low light.

Two patents have been issued in USPTO and PCT to protect this technology.

Mechanical design for the
first prototype camera system

5D SENSING

5DSENSING

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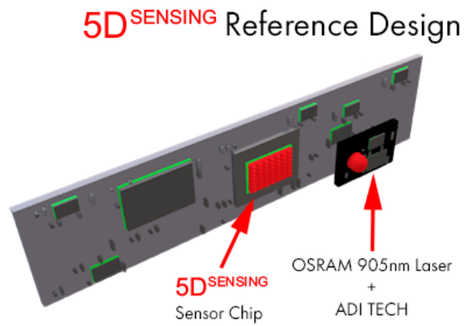
Business Model

5D SENSING focus on making and selling the CMOS sensor. With close support from the FAB, we will make a complete packaged and tested sensor. Our customers will be the camera makers that sell to companies who deploy the safe-city installations.

Currently we partner with an Asian company that will make the cameras for Asian markets.



Progress to Date

5D SENSING have demonstrate the Tx part of the system on hardware and finished the system performance model and simulations. We are now working to close the first round of 6M$ looking for making prototype chip and evaluation system by 2021.

Silicon Catalyst Start Date: 2020

Team

- Dr. Roni El-Bahar, CEO & Founder, experienced senior manager and scientist with over 20 years of relevant experience at Samsung, Intel and Huawei, CTO for Huawei Israel Research Center. Roni experience in products, technologies and research in the fields of optics, electro-optics, cameras, chip design and analog.
- Yaron Eldad, CFO, with 20 years of CFO and COO experience at international technology, biotech and trade companies. He led an IPO on NASDAQ and has been a CFO of NASDAQ traded companies.
- Niv Shwartz, business development, is the CEO & Founder of Shanghai Xinergy Global Business Consulting Co., Ltd. A company that supports western businesses in building their go to market plans for launching in China and raises capital from Chinese investors and government funds.
- There are additional 6 highly skilled technical personals on team (not full time)

Ask

5D SENSING has raised ~$500K through self-funding.

The company has secured seed investment that is sufficient for initial prototype phase and currently is looking for 6M$ series A investment. This investment should bring the company to a production-worthy sensor that can be generate customer revenues.

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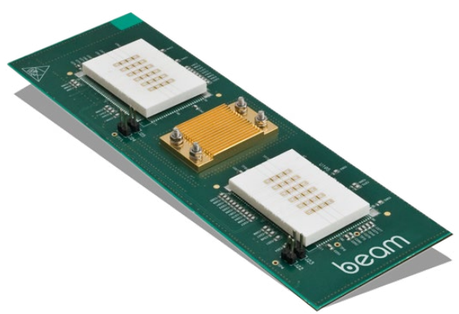
Beam Semiconductor

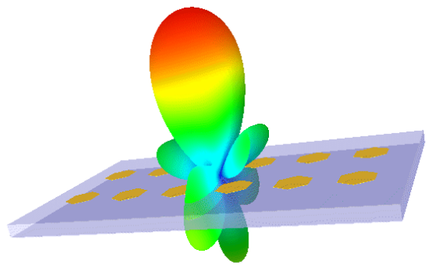
Wireless Backbone for the Mobile Internet

Overview
Beam has developed innovative RF silicon and unique antenna technology to address demanding 5G wireless infrastructure applications such as cellular backhaul, fiber extension and broadband / fixed wireless access last mile.

Problem
Demand for mobile bandwidth has undergone exponential growth under the pressure of smartphone video streaming (live / on demand) and gaming. IoT, V2V / V2X and innovative mobile apps are driving the push towards the next generation network ... 5G. Optical fiber is the technology of choice for gigabit network rollouts. However, fiber is costly, time consuming to install and impractical in many locations.

Solution
Beam's goal is to augment, extend and replace fiber with a compact broadband wireless transport solution based on patented 60 GHz and 28 GHz transceiver technology coupled with patented phased-array MicroHorn antenna technology. Beam has accomplished the integration of complex 3D internal structures in its MicroHorn antenna, forming a buried waveguide architecture that 'squeezes' the energy through it (much like a trumpet / horn) which provides power and gain. A point-to-point gigabit wireless link is formed with unique analog beam-steering RF electronics that allows the phased array antenna to automatically shape and steer the beam to eliminate manual positioning and achieve 10+ Gb/s throughput rates.





Market Size/TAM
- Global mobile wireless transport market @ $64B by 2025 with 13.52% CAGR
- Wireless transport silicon + antenna @ $2.8B in 2022

Beam Semiconductor

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Business Model
Depending on the application, Beam products include the full 5G mmW module (silicon + antenna), the standalone antenna or the RF silicon. Beam has focused on direct engagements with wireless OEMs and Service Providers. Revenue initially comes from NRE for engineering development services, followed by product sales.

Competition
Unlike consumer solutions such as WiFi and WiGig, Beam's proprietary 60 GHz platform is optimized for outdoor infrastructure applications and delivers superior data throughput, range, immunity to environmental variance, and reliability, resulting in robust link performance. Compared to existing microwave wireless solutions, Beam provides a dramatically smaller form factor, and its automatic beam steering sharply reduces cost.

Defensibility
Beam holds 8 US and international patents surrounding key aspects of its intellectual property involving analog beam steering, manufacturing of the MicroHorn antenna along with use of Beam's phased-array antenna technology for future RADAR (proximity / imaging) applications.

Milestones
- Strategic financial investment from Sanmina Corporation. Signed LOA which includes joint engineering development, manufacturing and Tier 1 wireless OEMs (Nokia, Ericsson, etc.) customer engagement.
- Pre Series A investments from the Band of Angels and KYTO Technology Fund.
- Won $600K grant from the SIIRD Foundation (Singapore Israel R&D) to develop 2nd generation 60 GHz module to address emerging China and India 5G markets.
- Telecom Council Innovation Showcase 2020 Class Member.
- In development: 28 GHz modules. 4x4 array and 16x16 array with multi-beam capability.

Silicon Catalyst Start Date: October, 2019

Team
- **Stacy Joseph**, CEO (Silicon Optix, Quicklogic, Texas Instruments, IBM)
- **Rafi Popovich**, CTO (ELTA, General Microwave)
- **Avigdor Berlin**, COO (Israel Aerospace Industries, ELTA)

Board of Directors
- Sri Purisai (Microsemi, California)
- Danny Spritus (Gilat / Raysat, Israel)
- Don McDougall (GLH, Canada)
- Stacy Joseph (CEO, Canada)

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California Mem Tech

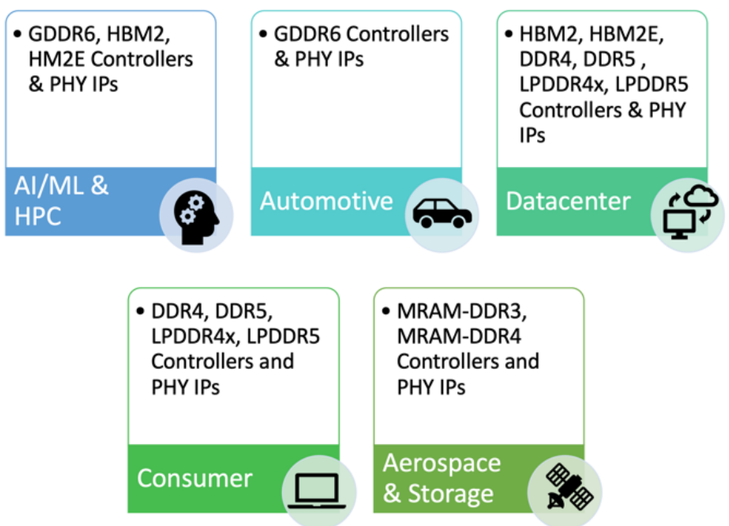
Future is already here

Company Overview
MEMTECH is a memory solutions company providing world's smallest DDR(Double Data Rate) SDRAM Controllers, PHY IPs, SDK Kits and Firmware using proprietary technology for AI/ML & HPC, Data centers, Automotive and Consumer markets.

Problem
DDR IPs contribute to huge increase(about 30%) in SoC die size. As a desperate measure, SoC providers are compromising on features and going for latest nodes. Limited availability of custom features making it difficult for SoC providers to create product differentiation. End result is a Commoditized SoC. SoC providers are not able to explore new market opportunities.

Solution
Our unique architecture gives us the advantage of building smallest design ever (30%-50% smaller than the competition). 300+ custom features in Controller and PHY combined for most applications. Niche product offering. Memory solution for Persistent memories like MRAM-DDR3, MRAM-DDR4 etc. Creating opportunities to explore new markets and stay ahead of the competition.

Markets and Products
Total Addressable Market for 2020 after correction for Covid is $897M. Since MEMTECH is currently focused on TSMC 12nm, its target market size is $224M.



California Mem Tech

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Competition
MEMTECH's competition mostly comes from established players. These solutions require a huge die size, higher cost and always associated with other EDA tools and services. Customers have confirmed that MEMTECH is the only place where fully integrated solution is available.

IP Support Ecosystem
A dedicated Application Engineering team, foundry support , customer support tools (JIRA) for tracking and visibility. Design reviews at various stages of the product development.

Resources
- Design Guidelines
- Routing Guidelines
- Reference Floor Plans
- Other resources to reach your goals fast.

Models
- Simulation Models
- SI Models
- Reference EDA flows and others to start implementing from day one.

Dcouments
- User Guides
- Register Documents
- Derivations of floorplans
- Documentation of entire EDA flow to jump start your design.

Training
- IP Basics
- Application Flow
- Features test
- Bring-Up flows
- Validation Plans trainings online or in-person.

Silicon Catalyst Start Date: May, 2020

Team
- Saswat Mishra, CEO, over 20 years at Apple, Intel, Huawei, Marvell, Synopsys, 20+ Patents pending
- Vasiliy Mikhel, CFO, over 20 years of experience in Management at Goznak, Independent Consultant
- Theodore White, Principal Architect, over 30 years of experience at US Navy, Q-Logic, Unisys and Marvell, 20+ Patents
- Michael Bartol, Principal, SoC Platforms, over 25 years of experience at Rodime, METS, Nohau and Marvell Semiconductor
- Sriharsha A, Principal , Analog Design, over 20 years of experience at Siemens, Marvell Semiconductor

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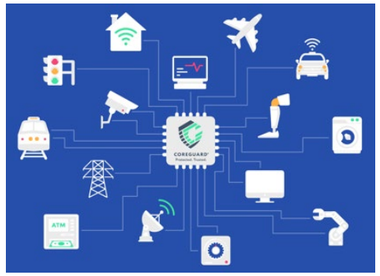
Dover Microsystems

Problem

Cybercrime costs are expected to hit $6 trillion a year by 2021. Historically, companies have sought to protect embedded systems by adding layers of defensive cybersecurity software. But this "solution" is not a solution at all. All complex software—including cybersecurity software—has bugs and these bugs can be exploited by hackers. The costs of cyber attacks are massive—debilitating remedial costs ($2.1 billion in the case of the recent Fiat-Chrysler Jeep hack), damage to corporate valuations, tarnished brands, and eroded customer confidence and loyalty. Companies are demanding more trustable and comprehensive cybersecurity solutions.

Unique Solution

Dover's CoreGuard® technology has its origins in a leading US Defense Department research program (DARPA) and was further developed at one of the world's leading research labs (Draper). CoreGuard is the only solution for embedded systems that can prevent the exploitation of software vulnerabilities and immunize processors against entire classes of network-based attacks. The CoreGuard solution is silicon intellectual property (IP) that puts security at the lowest possible level—in the silicon—where it cannot be subverted over the network. It is not hardware per se, but rather hardware design. It integrates with leading processor architectures to monitor every instruction executed to ensure that it complies with a defined set of security, safety, and privacy rules. If an instruction violates a rule, CoreGuard stops it from executing and prevents any damage from being done. CoreGuard's approach is unique and provides unprecedented protection to IoT devices. A CoreGuard technology license includes two components: hardware design files (silicon design IP) and firmware (instruction-based rules we call "micropolicies"). Because this firmware is small and is accessible ONLY by CoreGuard (and not by the host processor or the network), it is not vulnerable to attack.



Target Market

Dover's target markets include (a) device manufacturers in verticals who design and build their own system on chips (SoCs), including Industrial IoT, Aerospace, Communications, Automotive, and Medical Devices, (b) semiconductor manufacturers, and (c) companies that themselves license IP. The opportunity is massive, with our Serviceable Addressable Market exceeding $8.5 billion in annual revenue.

IP Business Model

Dover is an IP licensing company. We license the CoreGuard solution to customers making microprocessors and IOT devices. We also license CoreGuard firmware. Dover's revenue model consists of multiple revenue streams: evaluation licenses; up-front Design licenses: $1-3M; manufacturing licenses with per chip royalties; support and maintenance fees. Additional potential revenue post-deployment will include monitoring and analysis of highly valuable real-time attack data.

Strong Traction

Dover currently has multiple large customer wins and dozens in the pipeline. NXP, one of the world's largest semiconductor companies, is our first customer. Our contract is for a new processor for industrial and consumer IoT devices, which NXP expects will ship 300m units over 3 years. The total estimated contract value for this one part is $10 million. We expect

Dover Microsystems

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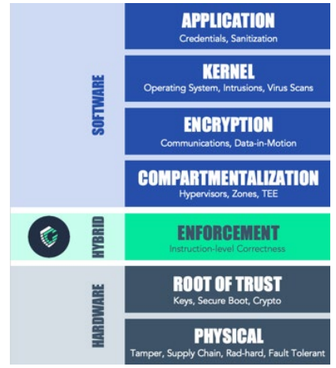
to have CoreGuard in additional NXP parts in 2021 and beyond. We have also signed a deal with Cadence, a leading electronic design automation (EDA) company, for joint-selling opportunities of their Tensilica processor IP integrated with CoreGuard. Dover has recently gained traction with the DoD, namely the Air Force Research Lab (AFRL), through a small defense contractor named Centauri. A project there valued at $2m will fund RISC-V based work that expands CoreGuard's micropolicy set. Additional projects for AFRL are in discussion as well. In addition, Dover has signed evaluation or partner agreements with several other companies and has three significant contracts expected to close in 2020.

Revenue & Projections

Since launching in July 2017, Dover has cumulative total revenue to date of $2.1m. Current projections are for $5m in revenue in 2020 (with pipeline to support this), and $16m in 2021 once first royalties start flowing. Dover's licensing model results in the bulk of project revenue coming 12-18 months after contract signature, after our customer delivers SoCs to their customers, triggering royalty revenue as well as service/maintenance fees. Royalties flow for at least 5 years and as much as 10 years with one SoC's royalty stream adding to all the previous ones making this a high margin, profitable, cash-efficient business model.

Competition

CoreGuard technology is a unique and disruptive cybersecurity solution for embedded systems-there are no other solutions like it on the market today. Its pedigreed development, deep investment, and robustness set it apart. However, the cybersecurity market is extremely crowded and noisy-with many claiming, but unable to deliver, "do-it-all" solutions. Dover needs to cut through all this noise to compete for security budgets. Typically, we see only two other approaches "compared" to CoreGuard: Arm's TrustZone product and encryption solutions from various vendors. Both are inferior to the comprehensive and robust protection of CoreGuard.



Competitive Advantage & Patents

There is a gap in the cybersecurity stack called "Enforcement." Everything above this level (compartmentalization, encryption, kernel, and application) is vulnerable to attack because it is based in software, and all complex software contains bugs. CoreGuard IP is the first and only solution to fill the Enforcement layer of the cybersecurity stack, providing what is called 'Instruction-level Correctness' and protecting embedded devices against 94% of known software vulnerabilities, including 100% of buffer overflows, code injection, and data exfiltration attacks. Our technology is the first of its kind to market, with a long head start over other hardware-based competitive solutions. CoreGuard technology is based on over ten years of development and $28 million of non-dilutive investment. It began as a part of a $100m US DoD DARPA program called CRASH, and then incubated at Draper Laboratory 2 years before spinning out as Dover Microsystems in 2017. Draper remains an equity holder in Dover. CoreGuard technology is protected by over 45 patents/applications that include both IP licensed from Draper and new IP developed by the Dover engineering team post spin-out. Dover holds an exclusive worldwide license to the IP developed while incubating at Draper.

Team

Dover's team of 15 highly experienced professionals is led by founder & CEO Jothy Rosenberg, a 9X serial entrepreneur and industry veteran. Jothy has extensive technology start-up experience, leading two previous start-ups to $100m+ exits.

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Eridan Communications, Inc.

The world's most efficient radios for 5G and beyond

Problem

5G is the next-generation wireless standard that increases bandwidth, supports more connections, and reduces latency, delivering the fast, ubiquitous connectivity to enable new applications from driverless cars to virtual reality. Yet by 2025, just 15% of all wireless connections are expected to migrate to 5G, because 5G base stations are too expensive and too power-hungry to deploy outside of dense urban areas.

5G base stations are currently 4x more expensive than LTE equipment, 3x as many are required for the same coverage, and they consume 3x as much power each. In an industry where revenue per user has been falling to flat for the past decade, the business case for 5G needs rewriting.

Solution

The Eridan MIRACLE Power Transceiver sends and receives cellular signals using 5-10x less power per GB transmitted, enables 2-3x cost savings for equipment, and provides 50-100x more data capacity in existing spectrum, rewriting the cost equation for 5G deployments.

By using gallium nitride in a switch configuration (not a linear amplifier), the MIRACLE can generate a more precise signal, use less power, and operate across all cellular frequencies (so it's tunable on the fly).

Market Opportunity

At scale, an Eridan MIRACLE transceiver can be in every wireless device on the planet. Including cellular base stations, mobile phones, connected cars, and connected devices, that's 3.7 billion units of addressable volume per year, and growing rapidly.

Competition

The MIRACLE replaces traditional power amplifiers used in concert with frequently proprietary transceivers and modems.

Business Model

Eridan is a fabless semiconductor company selling modules, subsystems and eventually Systems on Chip to equipment manufacturers, with additional revenue from design services and maintenance contracts for digital over the air upgrades.

The Eridan transceiver module will replace the power amplifier and digital-to-rf transceiver components of existing RF systems.

Eridan Communications, Inc.

The Eridan MIRACLE Transceiver Module

Progress to Date

Eridan is concentrating initially on two markets: defense and telecom equipment providers.

In the defense market, Eridan has received contracts from the DOD worth over $7M if exercised in full, with more in the pipeline. The defense market is relatively low-volume and price-insensitive, ideal for early production efforts.

In the telecom equipment market, Eridan has engaged with 3 of the 4 largest equipment manufacturers, and 3 of the 4 major United States wireless operators. Eridan has also seen substantial traction with small cell manufacturers around our value proposition of power efficiency.

Eridan is currently selling Developer Kits, which are laboratory demonstration models. Pre-production prototypes will be available in early 2021.

Silicon Catalyst Start Date: March, 2018

Team

Founded by 3 PhDs and serial entrepreneurs, company has grown to a team of 17 located in Mountain View and Croatia. CEO Doug Kirkpatrick is a former VC and Chief Scientist, DARPA.

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ESPRE TECHNOLOGIES

Espre Technologies

Chipsets, Modules, & Sensor Solutions for BoT & IIoT

The Product

Espre Technologies will offer chipsets, modules, and sensor products complementary to military BoT (Battlefield of Things) and commercial IIoT (Industrial Internet of Things) applications.

- **NVL-MIMO 1.0 (FPGA Chipset)** multiple antennas capacity, 5G equivalent scaling, global, terrestrial & aerospace communications applications.
- **NVL-AP WiFi (FPGA Chipset)** asset/vehicle mount, base station, LTE module, TCP/IP, UWB, regional communications coverage.
- **NVL-AP 200 (FPGA Chipset)** small form factor, light weight, wearable, asset/vehicle mount, close quarters communications.
- **NVL-Sensor 100 (ASIC Sensor Module)** small form factor sensor applications from wearables to Plug & Play applications with existing backhaul networks.

The Problem(s)

Security is crucial. Whether protecting troops, assets and military communications, or sensitive industrial transactions across the management platform, the loss of data integrity leads to losses on the battlefield and in the marketplace.

Capacity & Connectivity needs are increasing exponentially. As 5G becomes ubiquitous, hundreds of millions of sensors and billions of devices will compete for diminishing bandwidth.

Interference is everywhere. Competing sensors, devices and nodes all trying to transmit in real-time as well as increasingly mobile networks and topographical inconsistencies will degrade data efficacy and transaction delays.

The Solution

Security. Communication and data transactions are converted into patented, non-repeating, and random chaotic waveforms over encryption. Embedded Artificial Intelligence (AI) automatically identifies and digitally compartmentalizes threat attempts.

Capacity & Connectivity. The chaotic waveform(s) are tunneled beneath the noise floor of any wireless protocol (Wi-Fi, UWB, LTE, SATCOM, etc.) increasing network device connectivity and data capacity by tenfold.

Interference. AI driven optimized spatial diversity and spectrum allocations coupled with 10X+ simultaneous transactions compared to existing network communications minimizes multi-node and topographical interferences.

The Market

Over the next 5 years, the military/defense BoT communications market is expected to exceed $30B annually. The commercial IIoT market, excluding consumer-based routers and platform devices, will exceed $330B in 2020. Growing at a CAGR of 20%, the IIoT market will exceed $685B by 2025.

ESPRE TECHNOLOGIES

Espre Technologies

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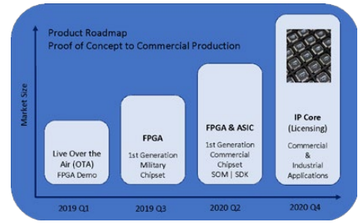
The Business Model



Espre will continue design and optimization efforts towards its initial suite of products under current military contracts. Final FPGA and ASIC chipsets will be transitioned into the commercial market(s).

Years 1-5, the company will contract with foundries to manufacture and deliver FPGA and ASIC chipsets and sensors directly to OEM consumers. By year 6, the company anticipates a transition to an ARM model where chipsets and sensors are designed in-house and licensed to OEM chip manufacturers to sell into their respective marketplace(s).

The Competition

There are several competing low bitrate, low-power, ad hoc network technologies including Zigbee, LoRa, and Zwave. The offerings are built on legacy technology and have been updated to target IoT applications. Predominantly suited to indoor coverage, they have well-known scalability problems and significant limitations on device/sensor connectivity. Outdoor centralized coverage suppliers, like SigFox, Ingenu, and NB-LTE, employ a cellular deployment approach requiring significant CapEx for physical tower and base station assets with a focus on wide-area coverage. While suited for asset tracking and fleet management, indoor coverage has diminished performance and suffers from topographical and device connectivity impediments.

Progress

Espre Technologies platforms and protocols are protected by 20 domestic and international patents. Currently operating under contracts totaling $1.8M, the company is augmenting its FPGA chipset and sensor designs to provide support for augmented reality applications like the ARMY iVAS (Integrated Visual Augmentation System). It is expected generated in $10-$12M revenue over the next 3 years.

Silicon Catalyst start date: October, 2018

Team

- Founder - Dr. John Terry, PhD.
- 4 FT Engineers - DSP, Communications, AI/Machine Learning
- 6 Subcontractors - Firmware Support, Antenna Design, and App Dev.

Investment

Espre Technologies is seeking $500K to complete our first-generation ASIC-based sensor products to support augmented reality applications for military/defense customers and wireless applications for Industrial 4.0.

Contact Dr. John Terry, john@espretech.com • +1 (703) 395-0257 • www.espretech.com

Mentium Technologies

Processors for complex video analytics on the Edge

Problem

AI inference acceleration at the Edge is a massive market opportunity

Mentium is focused on the very significant market of hi-end security cameras and drones where the need for intelligence has been on a surge. Moreover, COVID emergency is going to require even higher volumes and smarter capabilities for remote security and health monitoring.

Solution

Our solution is memory revolution: AI-Memory (AIM).
AIM is a computing memory chip that delivers unbeatable Neural Networks inference efficiency and speed.
We use a unique hybrid digital-analog architecture to deliver state of the art efficiency (20-50 TOPS/W) keeping a 10x in speed improvement.

AIM is a bolt-on chip for any existing system with a memory interface. It is the minimal hardware required to bring any system to world-class AI capabilities.

We envision a future where banks of AIM memory will work side-by-side with digital processor to accelerate AI algorithms in all kind of platforms.

Market Opportunity

"The global artificial intelligence chip market is projected to reach $91,185 million by 2025, growing at a CAGR of 45.4% from 2018 to 2025." (Allied Market Research)

Business Model

Selling IC product to system integrators and sub-systems suppliers, starting from hi-end Edge computing platforms such as security cameras.

Mentium Technologies

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Competition

Main competitors are:
Mythic-AI, developing a full SoC.
- Targeted at server and near-edge applications
- Architecture optimized for very big neural network models

Syntiant, came out with two products for trigger-words recognition on always-on microphones. These first products are fully-digital, as far as we know. They are working toward a mixed-signal SoC solution.
- Working toward SoC
- Directed at ultra-low power and ultra-small Neural Networks model for always-on audio application,i.e. tinyML (trigger words)

D-Matrix, developing full SoC
- Based on SRAM in-memory computation
- Limited by SRAM leakage
- Large area required, acceptable for server application

Mentium is not developing and SoC, but a minimal add-on directed toward mid-sized Neural Networks models that can enable complex real-time analytics on the edge.

Progress to Date

- We won a total of $1.1M in federal grants/contracts
- Added Paul Pickering to the team.
- Engaged with strategic partners.
- Third test chip taped-out initiated.
- New IPs filed across the whole chip design.

Team

- Mirko Prezioso, PhD, CEO, co-founder, semiconductor devices physics
- Farnood Merrikh Bayat, PhD2, CTO, co-founder, electronic engineering and comp. sci.
- Mark Ross, VPoE, veteran of semiconductor business, former Cypress CTO, System Architecture
- Jay Sulima, CMOS Designer, electronic engineering
- Pete Rodriguez, advisor and Board Observer, Silicon Catalyst CEO, veteran of semiconductor business
- Paul Pickering, advisor, 30+ years of experience in semiconductor product strategy
- John LeMoncheck, advisor, former CEO of Cambrios
- John Bowers, PhD, advisor, full-professor at UCSB and multiple startups co-founder
- Dmitri Strukov, PhD, advisor, co-founder, full-professor at UCSB, pioneer of neuromorphic computing
- Konstantin Likharev, PhD, advisor, co-founder, full-professor at Stony Brooks University, semiconductor physics and Neural Networks

History

We incorporated in February 2017, after working on in-memory computing technology for 5 years, mainly within the UPSIDE project funded by DARPA.

Contact Mirko Prezioso, mprezioso@mentium.tech • +1 (805) 617-6245 • www.mentium.tech

Multifractal Semiconductors

Fully-integrated E-band mmWave front-ends in base silicon

Problem

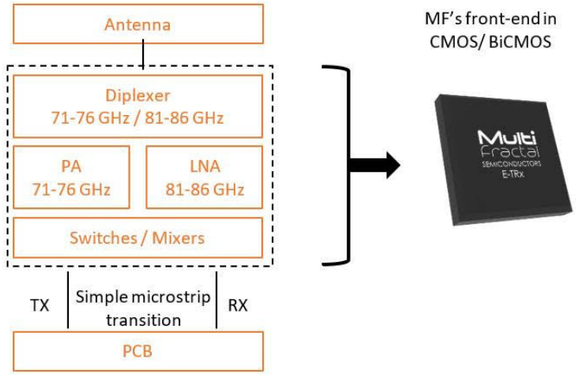
The IoT, or fourth industrial revolution, will see unprecedented volumes of data connect every aspect of the future connected person. The next generation 5G network will form the backbone of this revolution. The key enabling technologies of 5G are mmWave, small-cell densification & massive MIMO. The founders of Multifractal Semiconductors (MF) therefore believe that by 2030 the planet will be blanketed by E-band connectivity. Existing E-band front-ends are bulky (~size of shoe-box), expensive (~$11k), power hungry – and are not suited for mass production as required by small cell densification and massive MIMO.

Solution

MF is developing fully integrated E-band front-ends in base cheap & mass-producible silicon (CMOS/BiCMOS) to address this gap in the telecoms & automotive markets. MF's key enabling technology is the ability to create high-Q E-band filters (and diplexers) on-chip in silicon and integrate them directly (still on chip) with the LNA, PA, switches and mixers, all in cheap mass producible silicon (see figure below). Our customers can then feed the output of our IC directly into the digital back-end, reducing their front-end design, size, cost and effort. They do not have to worry about the RF – we do all that for them! This will enable miniaturization of the entire E-band front-end, for the first time allowing E-band small cell and massive MIMO.

Market Opportunity

The global mmWave technology market is at an early growth phase and was valued at USD 0.57 billion in 2017 and is expected to reach USD 4.08 billion by 2023, at a CAGR of 38.85%, over the forecast period (2018-2023)[1]. The E-band market is expected to dominate the mmWave space[2]. In 2017 Siklu sold approximately 10,000 links at the retail cost of approximately 10,000 USD per link. That is a single customer market size of 100 million dollars. We estimate, based on 2013 data, that Siklu has a market share of 25%[3]. This would place the total available market (TAM) for 2017 at 400 million dollars. The CAGR for the E-band space is about 38.85%[4]. Using this we extrapolate the TAM for E-band until ~2030: $2.8 billion in 2023, $5.5 billion in 2025 and $40 billion in 2030.



MF's target markets are subdivided into: telecommunications (5G backhaul, fronthaul, anyhaul, point-to-point, sat-to-ground) & automotive (radar). We plan to enter these markets as a fabless Silicon company by selling physical ICs to IDMs (Nokia, Siemens, Ericson, Siklu, NEC, Fujitsu, etc.). We expect to sell between 0.5 and 2 billion units (in telecoms) and 10-100 million units (in automotive) over a period of 10-15 years (worst-case – small cell and massive MIMO will make demand much, much larger). Each IC will sell for $20 (currently the equivalent (not on-chip) costs ~200 USD). The above translates to capturing 3-6% of the E-band market share (if we only reach 20% of the expected sale units) (worst-case scenario).

Multifractal Semiconductors

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Business Model

The first three years (until 2023) of our operations will focus on lean technology development as well as business development. During this time, we will be in constant contact with potential customers, to understand their needs and tailor our front-end IC for them. During our development cycle we will regularly ship sample ICs to our customers to validate requirements and allow them to adapt their product roadmaps appropriately (Siklu for instance is already expecting samples from us). The following years will see a ramp up to full production.

Competitive Landscape

Existing E-band IC front-ends (Infineon BGT80, Analog HMC7586, TI AWR1243, TuskIC, Anokiwave) lack integrated filter(s) which leads to the need for IDMs to design external filters in the microwave assembly (IMA), increasing size and cost. Reducing cost and size and enabling mass production is key (small cell / massive MIMO). Moreover, massive MIMO (>4000 front-ends) needs tight integration - SoC. Multifractal's value add lies in integrating the entire front-end on chip in base silicon as a SoC. The enabling technology for this is on-chip high-Q filters.

Progress to Date

- 2014: research begins at the University of Pretoria (MEng, PhD Eng degrees)
- 2017: proof of concept and incorporation of MF
- 2018 (Q1): GAP ICT & Telaviv SA winner ($20k)
- 2018 (Q4): SAAB defence NRE project ($25k)
- 2020 (Q1): TIA seed cash funding of $1.22M confirmed
- 2020 (Q1): Silicon Catalyst full in-kind support confirmed
- 2020 (Q2): Co-operation signed with Siklu to provide them with IC samples

Team

- **Joe Valliarampath**, CEO - PhD Eng, Nokia Siemens Networks (2 years), Denel Dynamics (5 years) as senior guidance and control system engineer, SAAB Defence (6 years)
- **Piotr Osuch**, CTO - PhD Eng, previously MWR InfoSecurity as security researcher (3 years), Delphi / Aptiv as concept engineer for LiDAR, SAAB Defence as RF/MW engineer (2 years).
- **Nish Singh**, MMIC Eng. - MEng, previously 5 years of business management experience, currently at IMEC IDlab at UGent (5G-PHOS - 5G integrated Fiber-Wireless networks).
- **Flavien Minko**, MMIC Eng. - PhD Eng, previously South African National Space Agency (4 years).
- **Marno van Rooyen**, MMIC Eng. - MEng, previously SAAB Defence as RF/MW engineer (7 years).
- **Hendrik Nel**, MMIC Eng. - MEng

Ask

We have secured seed funding of $1.22M (cash) as well as Silicon Catalyst in-kind support. A further $250-500k is sought to reduce risks and reduce time to market.

Contact Pretoria, South Africa • info@multifractalsemi.com • www.multifractalsemi.com

Owl Autonomous Imaging

The smartest choice for the road ahead

Company Description

Owl Autonomous Imaging, has created a new sensor modality: Intelligent 3D Thermal Ranging Imagers. For application in Autonomous things and more, these imagers perform in all-weather day or night to deliver safe autonomous operation.

Pain Points

The most determinant variable in the robotic mobility market will always be safety. Manufacturers will continuously be tasked with determining which technology solutions most effectively mitigate liability risks and cost for safe operation. Sensor technology must: (1) See through RAIN, FOG, SLEET, SNOW & EXHAUST, (2) Classify living objects (pedestrians, cyclists & animals) from inanimate objects, (3) Track high speed objects in front and to sides while delivering object velocities (3D), (4) Discern objects in shadows, intense glare at both near and far distances (HD quality). No sensor has been demonstrated that addresses these pain points. Additionally, Intelligent 3D thermal imaging is the ideal modality for thermal fever monitoring, test and measurement and security applications.

Solution

With 15 patents already issued, Owl's always on 3D Thermal Ranger provides HD imaging and precision ranging with 100x the resolution of LiDAR, operates day & night, in all weather, definitively classifies; pedestrians, cyclists, animals and vehicles (either moving or stationary) all the while calculating position, direction and speed (3D- true velocity) to unlock safe autonomous operation.

Technology

The foundation of our technology is an adaptation of a thermal imaging solution we developed under a challenge grant from the US Air Force to track ballistic missiles in flight traveling at over 1,000 mph. Our new low cost automotive camera fuses Thermal Imaging with Range (X,Y,Z). The heart of our camera is our proprietary digital focal plane array coupled with light field optics.

Defensibility

No other company has demonstrated a single imaging camera with X,Y, and Z for automotive applications at commercial price points (at 50x cost savings) and we do this using thermal imaging (completely passive). We have an extensive patent portfolio awarded (15) and pending (7) for multiple key technology components. We hold foundational patents for fusion, 3D velocity, focal plane array, optics, spoofing, all specific to the automotive solution.

Owl Autonomous Imaging

Go-To-Market Strategy

There are 3 distinct revenue related TTM market scenarios: Fever Detection and Industrial markets with a TTM of now to 2 yrs. Industrial supports moderate volume with price points of $10K, while fever detection supports high volume at $7K price points. TTM for Fleet Services (robotaxi) is 1 to 2 yrs with price points of $1K at moderate volume. Finally, Auto is ultra-high volume with $200 price points and a TTM of 3 to 5yrs.

Business Model – (B2B)

Owl sells imagers for the autonomous things market this includes associated 3D software stacks with annualized maintenance. Smart city solutions include fever detection and security.

Competition

FLIR is the largest supplier of commercial and industrial 2D VGA imagers. With their roots in Government & Defense, FLIR has diversified into 10 unique markets for non-defense applications with total sales in these commercial and industrial markets of $1.1B. Despite FLIRs market leadership position their market penetration is low with 5% market share in Industrial and 8% market share in commercial. The market for Autonomous things and Smart Cities is nascent and open to new entrants.

Milestones

- Proven and shipped product to US Air Force 2017.
- SHIPPED MVP Oct. '19, Traction: 2019 revenue of $850K.
- Shipping to Honda, and Hitachi for Auto, Movano for Security, example near term pipeline opportunities
  include ITRI (AV Bus), Cruise (robotaxi), Deutsche Bahn (people counting) and more.

Team

- **Chuck Gershman**, CEO, co-Founder, 30+ yrs, Exec Mgmt, Semi, Microsemi, Bay Microsystems, LSI, TI
- **Gene Petilli**, CTO, co-Founder, 30+ yrs, Digital Imaging, Kodak, Intrinsix, co-inventor of 1st optical scanner,
  co-inventor of the digital camera

Advisors

- **Pete Rodriguez**, CEO Silicon Catalyst, VP & GM NXP, CEO Exar
- **Sanjay Jha**, Former CEO Mot Mobility, CEO GlobalFoundries, COO Qualcomm

Contact Pleasanton, CA, & Rochester, NY • chuckg@owlai.us • +1 (510) 290-0195 • www.owlai.us

Power Down Semiconductor, Inc.

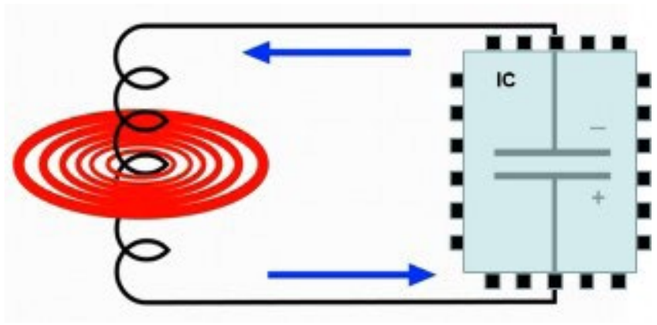
Energy-Efficient Solutions for Portable Applications

Problem

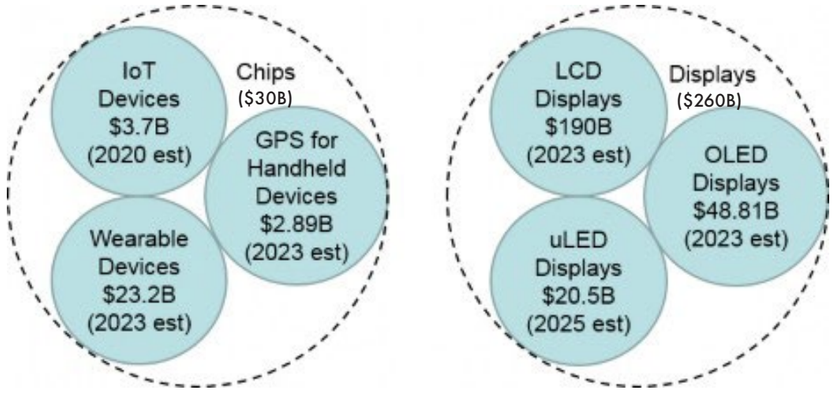
Today there is an ever-increasing demand for portable devices with extended battery life as well as greater performance. However, the supply is being limited by the efficiency of the processors and displays that comprise two of the largest energy consumers within those portable devices.

Solution

In response to the power-efficiency dilemma facing manufacturers of portable consumer electronics, Low Power Processing (LPP™) was developed. The technology uses a "pseudo-adiabatic" technique to recycle charge and prevent CV2f losses in memory blocks, clock buffers, GPIO, and displays.



Market Opportunity



Business Model

Direct Sales + IP Licensing: PDSemi designs and develops ICs for the IoT market. Chips are sold through local distributors in China. For IP model, companies license LPP technology and PDSemi receives a licensing fee for each chip or display sold. OEM will pay "10% of the benefit" as the licensing fee.

Power Down Semiconductor, LLC.

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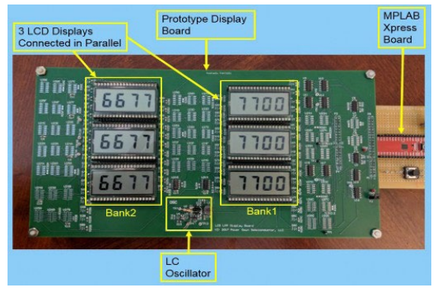
Competition

CLEARink Displays, Inc. – developer of low-power reflective displays that are an alternative to OLED, LCD, and E-paper with limited frame rate and color depth.
Eink, Inc. – developer of ultra-low power displays for E-readers with static images. Full-motion video is currently not possible.

Progress to Date

Two LPP prototypes built and tested. The SRAM chip shows a 25X reduction in power. The LCD display board shows ~30% reduction in power consumption over the traditional non-LPP prototype board.



Team

- **DH** - Founder & CEO, technical lead and/or manager on various high-reliability IC's for spacecraft & medical applications, A/D's, D/A's, References, Linear Oscillators, Sensor I/F IC's, Fiber Optic CDR's, PLLs for clock and timing applications.
- **FL** - President of China Division, co-founder of several technology companies in the US and China. Industry expert in OLED display development. Currently, professor at Suzhou Institute of Nano-Tech and Nano-Bionics. He is listed as inventor or co-inventor on over 100 US patents.
- **PK** - VP Sales and Business Development, various sales and business development positions including VP of North American sales for a Fortune 500 semiconductor company.
- **GK** - VP of Engineering, various technical leadership positions in high-speed semiconductor design – regarded as an expert in his field with several patents and publications.
- **LL** - Sr. Analog Designer, wireless RF design, LNA's, Mixers, VCO's. High-speed wireline equalizers, TIA's, and display drivers.
- **BY** - VP of Manufacturing, fabless IC manufacturing consulting, wafer fabrication, packaging, and test planning.

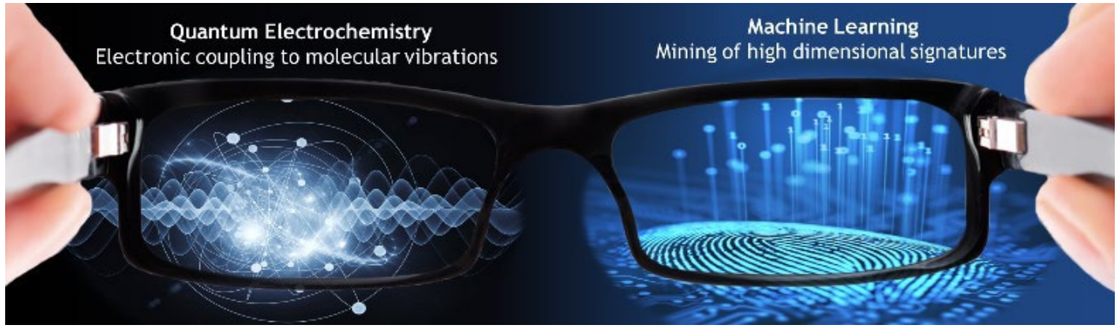
Ask

PDSemi has raised ~$400K through self-funding & 1 seed round. We are currently developing an ultra-low power 16-bit MCU for energy harvesting IoT applications. We are seeking $6.5M for the follow-on 32-bit ultra-low power MCU.

Contact David Huffman, dhuffman@powerdownsemi.com • +1 (408) 612-5257 • www.powerdownsemi.com

Probius Dx

Phenotyping biology at the quantum level



With a vision to decentralize and dematerialize clinical diagnostics for personalized health monitoring, ProbiusDx has developed a bioanalytical platform that brings the unique integration of multiple scales of biological information to simultaneously identify and quantify small molecules, large molecules, single cell organisms and their interactions in any background matrices. Using quantum bio-electrochemistry, our multiscale phenotyping platform increases the amount of accessible information by a factor x1000 and can be performed in the background matrix directly, without sample preparation and in limited sample volumes. Short term, it enables broad-spectrum and efficient longitudinal studies for pre-clinical therapeutic discovery and validation. Longer term, it will revolutionize healthcare by enabling individuals to monitor their biochemistry as a personalized baseline and close the loop between the patient, their doctor and their care provider digitally and in real time through a unique SaaS delivery model one could refer to as Diagnostics-as-a-Service (DaaS) or On-demand diagnostics.

Initial Go To Market:

$12B biomarker and assay market for preclinical R&D where we accelerate discovery and translation (PTM, TDM, drug distribution, stratification). Our differentiation from incumbent mass spec and binding assay based multiplexing technologies is our unique broad-spectrum and multi-scale phenotyping capability, the small sample volume and the highly multiplexed software defined assays integrating matrix effect/phenomics in a greatly simplified and more reliable workflow.

Probius Dx

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"If you want to find the secrets of the universe, think in terms of energy, frequency and vibration" Nikola Tesla

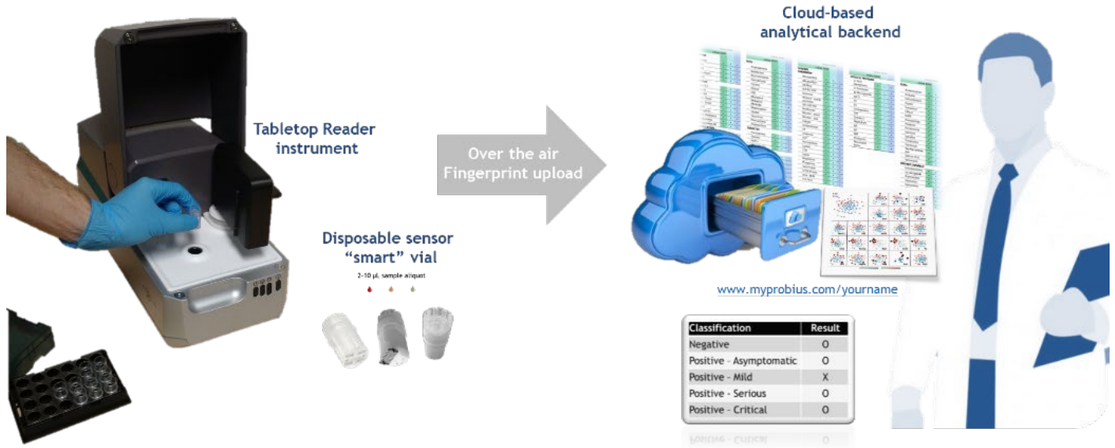
Technology: 3 Main Elements

- A disposable "smart" vial with embedded chip scale sensors which encode specie vibrational information of complex samples into an electronic signal using a quantum electrochemical transduction approach.
- A state-of-the-art electronic readout instrument which scans the vibrational energy of all molecules within the sample to integrate all available information into a high dimensional fingerprint.
- A cloud hosted software backend which pixelates the unique sample signature into a digital twin and compares with pixel signatures of available references (blank target, clean matrix, spiked target) to infer presence and concentration of any target via machine learning and classification algorithms, in quasi real time or a posteriori.

History and Status:

- Spun out of Stanford in 2016 with exclusive rights to intellectual property with no restriction
- $3+M in non-dilutive funding (DARPA) and $2.5M seed round (Baidu, TSVC, Shanda Group, Joyance, StartX, SHA)
- 6+ signed pilots (Astra Zeneca, Merck KGaA, Denver Health, Biorad, BASF, Harvard BWH) and many others in backlog
- Raising $10-15M series A to support the preclinical solution launch in 2021 and scaling of our high profit margin DaaS model.

From "lab at the edge" to "sample digital twin": The DaaS workflow



Contact: Emmanuel Quevy, emmanuel.quevy@probiusdx.com • +1 (510) 827-5604 • www.probiusdx.com

Quadric

Supercomputing At The Edge

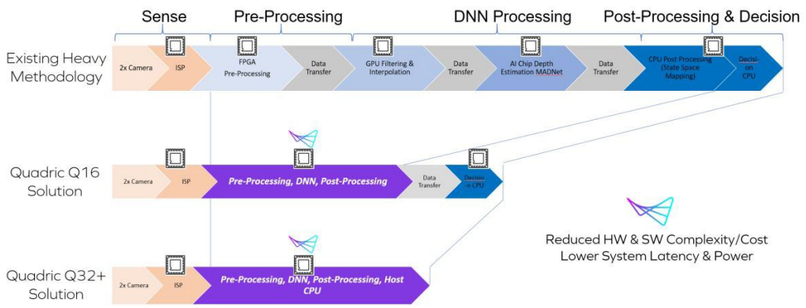
Problem

Quadric has built a full-stack system that is designed to meet the latency & power requirements of next-generation edge com[uting products. The magnitude of data generated by edge solutions is estimated to reach totally unmanageable proportions of 175 Zetta Bytes by 2025. This is too much data to process in the cloud due to latency, bandwidth and privacy concerns. In order to handle these data volumes, the next generation of innovation in computing will happen outside the data-center and closer to the Edge. Quadric has created a solution that is specifically optimized not only for Artificial Intelligence (AI) workloads, but also for Image Processing, Data Analytics and more.

Solution

Quadric's built a unified processor architecture where developers have the power to write and unify all parallelizable algorithms onto a latency-optimized processor. Unified Compute gives the developer power to accelerate works onto a single cohesive software Compute gives the developer power to accelerate works onto a single cohesive software and frameworks.

The Quadric Processor replaces a host of components with a single latency, performance, and power optimized processor architecture. All software workloads previously running on those hardware components. Including but not limited to: DNN, CNN, LSTM, Path Planning, Pre and Post Processing, Filtering, FFT, BLAS (GEMM, GEMV, AXPY), Sorting and Classical CV) now run on Quadric processors.



Business Model and Markets

Quadric licenses its compiler software along with selling accelerator cards, chips & IP for performing AI as well as traditional HPC workloads in the following markets:

- Industrial IoT & Sensor processing Edge servers
- 5G base stations
- Smart City and Smart Home appliances
- Security/Video appliances
- Autonomous vehicle: sensor and ADAS
- Medical imaging equipment

Quadric

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Progress to Date

- **Seed & Series A**: Quadric has raised a total of $15M since 2017
- **Software & Hardware Architecture**: Quadric completed the design & prototyping of the first version of compiler software as well as patented hardware architecture in 2019
- **Announced Partnerships**:
  - Denso/NSI-TEXE: For autonomous vehicle and industrial robotics
  - Cybertrust/Softbank: For edge servers in premise industrial IOT and 5G
  - TSMC, IMEC, Synopsys, Cadence
  - Silicon Catalyst start date: 2019
- **DNN Compiler & FPGA Kits**: Quadric is currently shipping FPGA kits along with HPC compiler software supporting DNNs along with pre/post processing of data
- **Key upcoming milestone**: Tape-out of the first Quadric processor in July-2020

Silicon Catalyst Start Date: 2019

Team

- **Veerbhan Kheterpal**, CEO & Co-founder, Founded three technology companies w/ two acquisition exits. Full stack expertise from Software to Silicon across Datacenters to consumer facing products. Ph.D. & M.S in ECE from Carnegie Mellon University.
- **Nigel Drego**, CTO & Co-founder, Prior to Quadric, Chief Architect & Co-founder at 21, Inc. where he designed and built-out three generations of mining ASICs. Full stack expertise from Software to Silicon. R&D at PDF Solutions & Intel. Ph.D. EE from MIT.
- **Daniel Firu, CPO & Co-founder**, Prior to Quadric, Daniel co-founded handled microarchitecture and physical implementation and manufacturing of 21's first chips. He led business development efforts for licensing 21's Bitcoin-related IP. M.S, ECE from University of Florida.
- **Tim Smith**, Tim is a respected semiconductor industry figure who has managed, negotiated, and delivered numerous high value multi-year, multinational, collaborative business engagements consistently increasing sales and profit. He has led Sales & Business Development at several companies eg. Rambus, IntinsicID, CoWare, Sonics, Tiscend and was the founder and Managing Director of Memec Design Services.

Ask

We have expanded the applicability of our platform to several new domains. Currently, we are taking in new customers in the area of real-time analytics in IOT, manufacturing & healthcare use cases. Customers can tremendously reduce bandwidth and cloud resource utilization by deploying on Quadric's edge computing stack.

Contact Tim Smith, tim@quadic.io • +1 (408) 898-6318 • quadric.io • Linkedin, Twitter: @quadric_io

Seamless Microsystems
Digitizing Your World Seamlessly

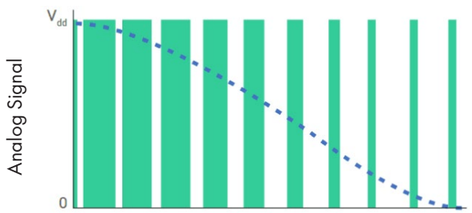
Seamless Microsystems

Problem
Power and performance of analog circuits are the biggest bottle-neck for next-generation systems

Opportunity
High-performance analog design has seen NO fundamental disruption in 50 years

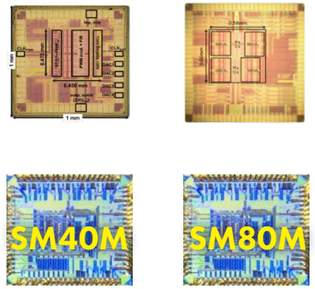
We fundamentally reimagine analog design using patented time-domain techniques.

Switched-Mode Signal Processing



Pulse-width encoded signal

- Pulse-width based analog design using switches
- Performance improves with CMOS scaling



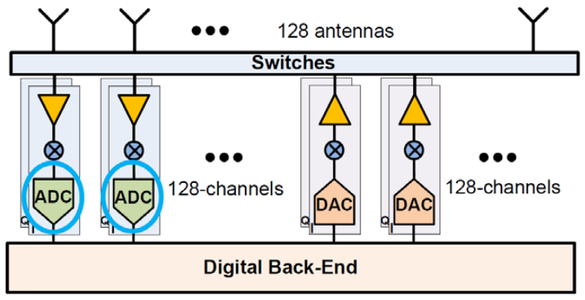
Si-proven in multiple chips at 65nm and 28nm

Automotive (Our Present)
Delivered analog front-end to customer

Medical Imaging (Our Past)
Developing the best data converters in sensors for a major customer

Communications (Our Future)
Integrated data converters and Power Amplifiers for base-stations

Example of the Seamless effect in 5G base-stations (BTS)



Them
1W/ADC
128W/BTS

Us
0.2W/ADC
25.6W/BTS

5X lower power ADCs for 5G BTS

Seamless Microsystems
Digitizing Your World Seamlessly

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Seamless Microsystems

Revenue Model: Chips, Die/Chiplets and IP Licensing

Short-term: IP core Licensing
- For medical and automotive industries first customer in medical imaging
- $MM deals with international automotive companies

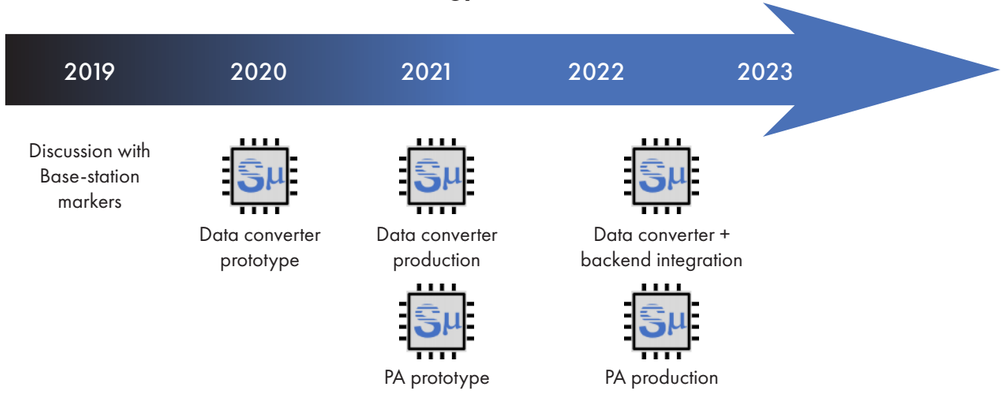
Long-term: Chips and Die/Chiplets
- For communications
- Discussions with base-station providers to define specifications

Competition

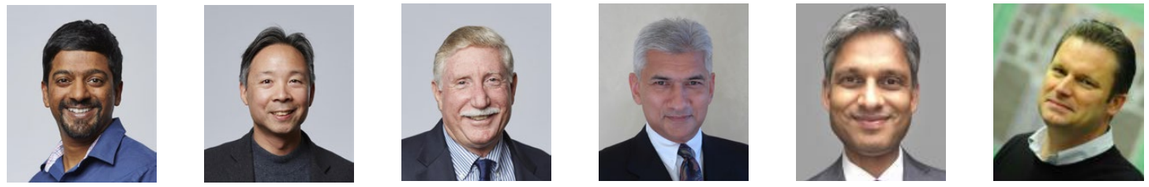
Chip Makers: Analog Devices, maxim integrated, Texas Instruments

IP Providers: SG Group, cadence

Go To Market Strategy for Communications



Team



Jayanth Kuppambatti
CEO

Augustine Kuo
VP of Engineering

R. Scott Hills
VP Sales

Keith Lobo
Business Advisor

Vipin Tiwari
Executive Advisor

Peter Kinget
Technical Advisor

Contact Jayanth Kuppambatti, jayanth@seamlessmicro.com • www.seamlessmicro.com

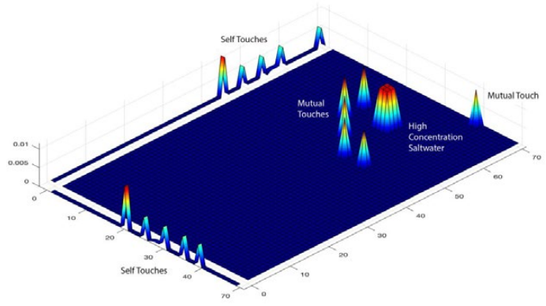
SigmaSense

Overview
SigmaSense®, the global leader in touch sensing performance, is changing the world of traditional analog sensing with a new advanced digital approach. By providing concurrent modality, applying efficient digital filtering, and greatly improving noise immunity, SigmaSense is delivering over 100X improvement in performance. Products ranging from small wearables to greater than 100 inch displays can now provide a superior human interface sensing experience that also reduces system costs and lowers design risk. Headquartered in Austin, TX, SigmaSense provides semiconductor and board level products with development tools, advanced software drivers and support.

Markets
SigmaSense is providing smart touch screen controller technology to the $150+ billion display industry, representing opportunities of more than $5 billion today. The Company is also developing a next generation of delta- sigma analog-to-digital converters (ADC), representing a $2+ billion opportunity across a range of IoT markets.

Customer Problems
Customers expect all screens to be capable of good predictable touch regardless of size. Display manufacturers are pursuing higher value by the integration of touch sensing into the display itself. Currently, large and/or flexible displays face a wide array of issues in supporting capacitive touch due to the varying high resistance and capacitive loads, RC timing constraints, and environmental noise. Current technologies are simply not up to the task and cannot provide the capacitive imaging or response times now demanded for interactive displays.

Problem Solved
SigmaSense is pioneering the massive shift to low power multi-frequency concurrent modality for analog sensing systems. With its unique and patent-protected IP, SigmaSense is delivering a variety of sensing solutions to provide 100X improvements in touch performance while enabling new user experiences through SigmaVision™ capacitive imaging. The result is unparalleled performance, new capabilities all combined with reduced design cycles and nearly instant tuning / calibration efforts.



Proprietary Core Invention
When communications evolved to support concurrent talk and listen the world changed in significant ways. SigmaSense delivers concurrency at the edge between analog and digital which enables a new generation of sensing with far better SNR with instantaneous results. SigmaDrive™ provides ultra-low voltage multi-frequency

SigmaSense

SigmaSense

generation and sensing with concurrent drive, sense and comms on a single pin. SigmaDrive technology concurrently drives AND senses, transmits AND receives, instantaneously detecting and adapting to any change of impedance in a sensing system. The most common customer reaction… “This Changes Everything”.

Capacitive Imaging
Capacitive-Imaging utilizes the SigmaDrive™ Architecture to deliver an image of the entire display surface with energy efficiency and without the lag normally associated with PCAP based touch controllers. Traditional coordinate-based reporting cannot provide the rich data stream necessary to deliver the user experiences demanded by the market.

Competition
SigmaSense creates an entirely new class of touch controller performance. Current touch controllers must increase voltage and insert long delays in sampling to meet customer SNR requirements. Using customers’ existing systems for benchmarking, SigmaSense delivers performance that is 100-1000X better.

IP Protection
SigmaSense has substantial investments in its patent filings. The core IP around SigmaDrive™, displays, and Pen support are issued, additionally over 200 inventions are protected through placeholders. The patent filings extend to a range of applications beyond traditional touch screens, including power regulation, electric motors, data communications, medical, automotive and IoT applications.

Investment
To date, the company has raised more than $17 million from key strategic customers and angel investors.

Silicon Catalyst Start Date: October, 2019

Team
- Rick Seger, CEO
- Shawn Gray, COO
- Troy Gray, VP, R&D
- Steve Sedaker, CMO
- Gerald Morrison, CTO
- Gary Baum, VP Emerging Technology
- Rudy Prince, CFO
- Dan Van Ostrand, VP Engineering
- Nick Shamlou, VP Sales

Contact Rick Seger, rseger@sigmasense.com • +1 (512) 577-1235 • www.sigmasense.com

SPARK Microsystems

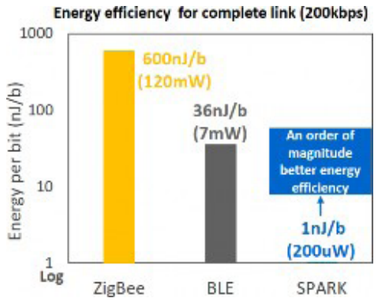
Wireless Without Compromise

Problems of Today's Wireless Technologies:

- The battery life of wireless devices is insufficient for many applications, leading to overly frequent recharge cycles, limited connectivity, and bulky batteries or costly maintenance. Ultimately, this is due to the inefficient wireless transceivers that are available on the market.
- Current wireless technologies significantly restrict the amount of data throughput and are not low power enough to enable continuous sensor data streaming using energy harvesting technologies.
- The long latency of wireless technologies makes their use inadequate in emerging new applications requiring real-time communications, such as AR/VR and Body Area Networks.

Solution

The SPARK Radio: Ultra-Low Power and ultra-low latency Wireless Communication that enables applications that cannot be addressed by existing wireless technologies, like battery-less sensor nodes, AR/VR, high-quality 3D audio, and dense, responsive and efficient networks.
The SPARK radio is a patented short-range (up to 100m) ultra-wideband wireless communication technology that provides an order of magnitude better energy efficiency and latency than competing technologies. It also enhances link reliability while offering a scalable data rate at up to 20 Mbps. SPARK has 22 patent filings and has 13 patents granted or allowed.



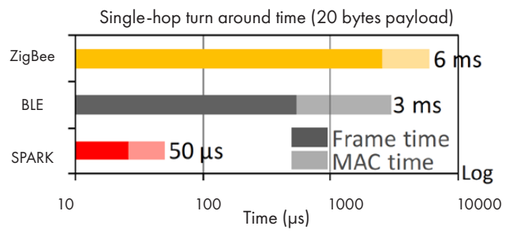
Market Opportunity

The low-Power wireless transceiver market is a $8B industry growing at a 14% CAGR. Typical solution providers require between 100k and 10M units per year. SPARK is involved in deep customer evaluations, Proof of Concept and prototypes designs in:

- AR / VR peripherals
- High quality 3D audio headsets
- Low power / latency gaming peripherals
- High-quality audio streaming and synchronization
- Low power high accuracy indoor ranging
- Physical distancing
- Smart assistants, homes, buildings

Other longer-term markets:

- Battery-less sensor nodes
- Industrial automation, M2M
- Smart agriculture
- Medical
- Automotive



SPARK Microsystems

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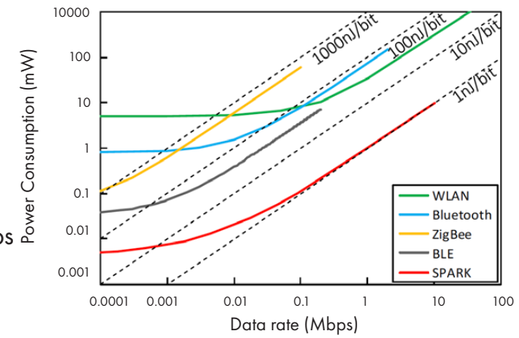
Business Model

SPARK Microsystems will sell an integrated circuit to product manufacturers and system integrators. SPARK may license its IP to select partners. SPARK targets penetrating the market by enabling compelling applications that were previously wired or compromised, then build a consortium of customers and partners to drive the next gen ultra-wideband standard.

Product Specifications

The SPARK radio achieves more than 15X – 40X more energy efficiency and 60X shorter latency than today's low energy technologies such as BT5 / BLE. It also features more reliable and secure high quality of service communication, while enabling data rates up to 20Mbps.
Main features are:

- < 10 µW at 1Kbps and < 1 mW at 1 Mbps
- 1 nJ/bit energy efficiency at data rates up to 20 Mbps over-the-air
- 1.8 to 3.6 V supply, 700 nA sleep current
- Ultra-short latency, 50 µs to transmit 1000 bits
- Ultra-low power Time of Flight (ToF) indoor positioning to within +/- 30 cm accuracy
- Ultra-low EMI and excellent coexistence with WiFi and BT



Milestones

- Q4 2016: Silicon Catalyst portfolio company
- 2017 through 2019: product enhancements from alpha, beta to pre-release silicon; customer evaluations and feedback across all stages
- Q1 2020: Closed post-seed SAFE; production tape-out & chip validated; launched product.

Upcoming

- Q2 2020: SVB venture debt; shipping production eval kits and pre-production volumes
- Q3 2020: Product qualification and characterization and volume ramp
- Q4 2020: Next gen SPARK transceiver MPW tape-out
- Q3 2021: Series A

Revenue estimates

$1M in 2020 ramping to $4M in 2021, and > $10M in 2022

Team

- **Fares Mubarak**, CEO, more than 30 years of semiconductor experience spanning ANSYS, Actel, Samsung and AMD.
- **Dr. Frederic Nabki**, co-founder & CTO,16 years of IC design and MEMS experience and in the technical management of R&D
- **Dr. Dominic Deslandes**, co-founder & CSO has 18 years of RF systems design, managed several antenna design, RF system integration and interconnections.
- **George Taylor**, VP Sales over25 years of semiconductor sales experience

Contact Fares Mubarak • fares.mubarak@sparkmicro.com • +1 (925) 998-7330 • www.sparkmicro.com

Teramics

Leading mmwave Solutions

Overview
Teramics has developed innovate mmwave GaN, GaAs, SiGe, InP, and SOI products to address the insatiable appetite for bandwidth in military, aerospace, satellite and commercial communication markets.

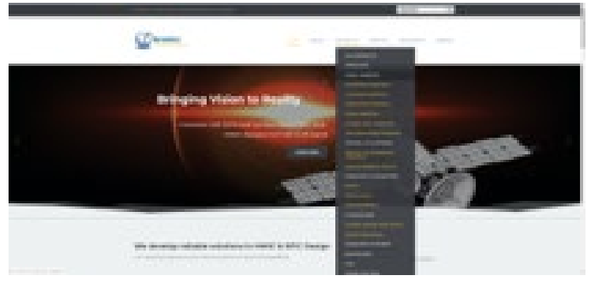
Opportunity
The exponential growth in data rates and the increasing need for bandwidth in applications such as 5G FR2, 400 Gbps PAM4, 76GHz ADAS, phased array radar present the opportunity for innovative highly linear and efficient products.

Solution
Teramics has developed the most linear and efficient power amplifiers in Ka/Q/V bands. Complementing these innovative power amplifiers are a variety of cutting edge mmwave solutions from Teramics such as low noise amplifiers, and up and down converters. Teramics is also offering integrated solutions for full mmwave phased-array products to be deployed in commercial, defense and space applications.

Market Size/TAM
The total available market for mmwave SSPA is $1.4B by 2025 with 9.4% CAGR.

Business Model
Teramics can offer complete mmwave solutions using a combination of its own mmwave GaN, GaAs, SiGe, InP, and SOI packaged ICs and off-the-shelf components. We will be able to address both niche applications demanding cutting-edge products such as SSPA for Space and high-volume markets such as 5G and ADAS.

Teramics



Competition
Teramics solutions are optimized for mmwave bands with cutting-edge performance. The linearity and efficiency specification of Teramics power amplifiers such at 20W at Q-band are second to none. Compared to existing solutions, our products have improved performance, smaller size, weight and cost and can be tailored to each customer needs.

Milestones
- Developed a portfolio of mmwave ICs, 2018
- Developed high power mmwave packaging, 2019
- **Developing integrated phased-array solutions, 2020**

Silicon Catalyst Start Date: June, 2020

Headquarter: Silicon Valley, CA

Founders
- **Seyed Tabatabaei,** CEO
- **Mona Molaasgari,** COO

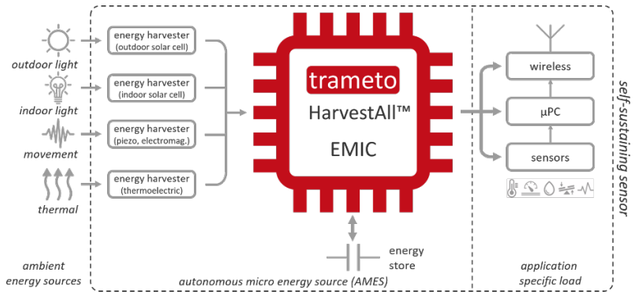
Board of Directors/Advisors
- **Anh-Vu Pham**
- **Richard Curtin**

Contact support@teramics.com • +1 (707) 849-2842 • www.teramics.com

Trameto Ltd

Enabling Battery-Free IoT

Problem



It is forecast that there will be 62 billion connected devices by 2024 and trillions of connected devices by 2030. This growth will be driven by industry initiatives such as tiny machine learning (tinyML). The usual definition of tinyML is running machine learning on embedded devices at an average of less than one milliwatt in power. This power requirement is important because it allows unattended devices running on batteries or energy harvesting. If we postulate that half of the 62 billion connected devices will be battery powered, and that of these batteries' half will need to be replaced every year, this equates to 60M battery replacements needed per working day, which is infeasible.

Solution

Micro energy harvesting, and the use of autonomous micro energy sources (AMES) – is seen as an ideal solution to creating self-sustaining sensor and tinyML systems. Along with energy harvesters and energy storage, the key component in an AMES solution is a Power Management Integrated Circuit (PMIC). Trameto's patent protected solution uniquely enables harvesting from any type of harvester, many instances of the same energy harvester or multiple types of different energy harvester.

Market Opportunity

In Energy Harvesting: Reaping the Abundant Market, Semico Research forecast that PMIC device sales for micro energy harvesting will grow to 1.2B units (2024) at CAGR 80%. Further PMIC growth will be driven by the market expansion, driven by initiatives such as Google led tinyML, of trillions of connected devices by 2030. Trameto is predicting revenues of $100M (2025) rising to $500M (2030).

Business Model

Trameto is a fabless semiconductor company, selling our device to system integrators within the industrial IoT. Our route to market will use reference designs and is via a blend of direct sales, distribution and manufactures' reps.

Competition

We have identified other suppliers of PMICs including TI and Analog Devices. All devices identified are defined, and limited, by their single input harvester capability. Clumsy and costly work-arounds are used for multiple inputs.

Trameto Ltd

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Progress to Date

2017
- Seed funding round closed

2018
- Japanese market introduction
- Euro Commission SME Phase1 grant
- Europe market introduction
- UK & USA Patents granted

2019
- Proof of Concept platform
- Smart Cymru grant
- Join Silicon Catalyst

2020
- Mark Ross joins advisor & tech contributor
- JDA leading harvester provider demo to customers
- Engineering sample T/O (July '20)

We have received letters of support from companies within the following sectors; machine condition monitoring, asset tracking, transport and smart buildings. We have also agreed a strategic partnership with a system integrator to further support commercialisation through evaluation of our devices. Other industry-leading companies have also committed to evaluate our first devices (engineering samples available fall 2020).

Silicon Catalyst Start Date: October, 2019

Team

- **Huw Davies**, CEO & founder has held executive and founder positions in the semiconductor industry from start-ups (Audium) to multinational corp. (Conexant Systems)
- **Laurence Strong**, CPO & founder, 25 years of technical marketing and electronic and design applications
- **Jon Oates,** CFO is an experienced financial controller, raising capital for technology start-ups and successful exits; part of the executive team at ICERA sold to Nvidia for $420M.
- **Mark Ross**, Advisor & Technology Contributor has been at the centre of the Silicon Valley working for companies like Dell, Cypress, Cisco Systems, and Sun Microsystems.

Next Steps

In Nov 2019, Trameto started a $3,200,000, 21-month project, which is part fund ed by a non-dilutive grant. We are looking to secure investment Seed-B (corner-stoned by current institutional investors, DBW). This next round of funding will unlock $1,250,000 of as yet unclaimed grant funding. During the next 18 months we will deliver engineering and pre-production samples of energy management IC and secure first customer orders.

Contact Huw Davies, huw.davies@trameto.com • +44 777 1790 112 • www.trameto.com

Zeno Semiconductor, Inc.

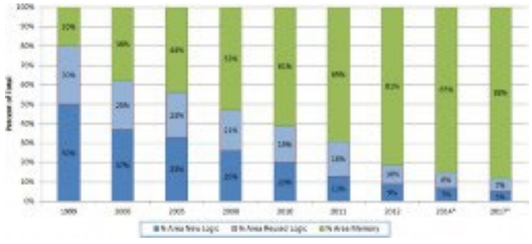
Brief Profile

Zeno Semiconductor, Inc. is a technology licensing company developing innovative scaling solutions in memory and logic technology. Zeno has been granted 100+ US and international patents.

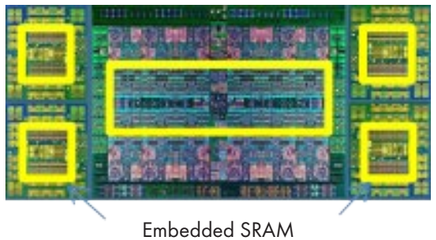
- Incorporated in 2010
- Silicon Catalyst start date: Oct 2016
- Funding: Angel, NSF SBIR grant, Corporate
- Stage: Silicon validation from major foundries across different technology nodes (14/16nm FinFET, 28nm, 40nm, 55nm)

Memory Technology: 1-transistor / 2-transistor Bi-SRAM World's Smallest SRAM Cell

Memory area on System-on-chip (SoC) occupies a significant percentage of total chip area, making embedded memory area and power efficiency a critical component in future IC designs. According to Semico Research Corp., embedded memory occupies >50% of total SoC area.

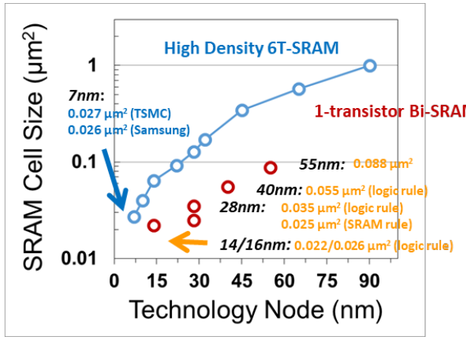


Source: Semico Research Corp.



Embedded SRAM

Conventional SRAM cell employs 6 transistors. Zeno Bi-SRAM is a novel static memory cell (no refresh operation) that offers 3-5x smaller cell size compared to conventional SRAM cell and is compatible with CMOS process.



Zeno Bi-SRAM cell at 28nm is smaller than 7nm High-Density (HD) SRAM

For more technical details, please see:

Han, Jin-Woo, et al. "A novel Bi-stable 1-transistor SRAM for high density embedded applications", IEDM 2015.

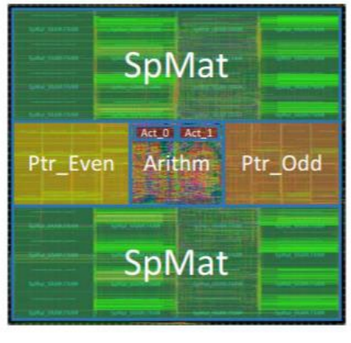
Widjaja, Y. et al. "A Bi-stable 1-/2-Transistor SRAM in 14nm FinFET Technology for High Density / High Performance Embedded Applications", IEDM 2018

Stanford

Zeno Semiconductor

Case Study: AI applications

Memory takes up a significant fraction of AI chip area and power consumption. The following example illustrates that memory occupies >90% area and 59% overall power consumption.



THE IMPLEMENTATION RESULTS OF ONE PE IN EIE AND THE BREAKDOWN BY COMPONENT TYPE (LINE 3-7), BY MODULE (LINE 8-13). THE CRITICAL PATH OF EIE IS 1.15 NS

	Power (mW)	(%)	Area (μm^2)	(%)
Total	9.157		638,024	
memory	5.416	(59.15%)	594,786	(93.22%)
clock network	1.874	(20.46%)	866	(0.14%)
register	1.026	(11.20%)	9,465	(1.48%)
combinational	0.841	(9.18%)	8,946	(1.40%)
filler cell			23,961	(3.76%)
Act_queue	0.112	(1.23%)	758	(0.12%)
PtrRead	1.807	(19.73%)	121,849	(19.10%)
SpmatRead	4.955	(54.11%)	469,412	(73.57%)
ArithmUnit	1.162	(12.68%)	3,110	(0.49%)
ActRW	1.122	(12.25%)	18,934	(2.97%)
filler cell			23,961	(3.76%)

Source: Han et. al., ISCA 2016

Using Bi-SRAM will result in significant area and power savings:

Area	38-47% of 6T-SRAM macro
Write Power	80% of 6T-SRAM
Read Power	20-25% of 6T-SRAM

Team

- **Yuniarto Widjaja, PhD**, CEO & Founder, PhD in Chemical Engineering with minor in Electrical Engineering from Stanford University in 2002
- **Zvi Or-Bach**, Executive Chairman, Serial entrepreneur with over 25 years of experience. Founder of Chip Express, eASIC, and Monolithic3D
- **Stefan Lai**, Former Intel VP, Co-inventor of ETOX Flash memory
- **Dinesh Maheshwari**, CTO of Memory Div., Cypress, Member of Board of Directors of JEDEC, senior technical positions at startups (acquired by Mentor Graphics and Cadence), invited papers in ISSCC and CICC
- **Prof. Yoshio Nishi**, Stanford EE, MSE, IEEE Fellow, 1995 IEEE Jack Morton Award, 2002 Robert Noyce Medal
- **Paul Lui**, President and GM of SST China, CEO of Linvex Technology (acquired by SST) and President (USA) of Macronix
- **Serguei Okhonin**, Founder of Innovative Silicon, ActLight
- **Pieter Vorenkamp** SVP of Operations, Broadcom, SVP and GM of IP Group, Cadence

Contact • 830 Stewart Drive #104 Sunnyvale, CA 94085 • +1 (650) 575-3555
contact@zenosemi.com • www.zenosemi.com

Portfolio Companies

ALUMNI

PROBIUS

Multi-scale biochemical phenotyping
in limited sample volume
www.probiusdx.com

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Providing the muscle to run Machine-Learning
and AI Algorithms on the Edge
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High Performance Integrated Optical Motion Sensor
for the Self-Driving Cars Market
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Silicon Catalyst Angels

EXPERIENCE ... THE DIFFERENCE

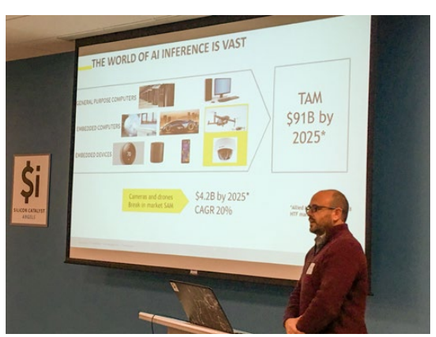
Silicon Catalyst Angels Board Members:
Raul Camposano, Amos Ben Meir and Michael Joehren

Silicon Catalyst Angels was spawned from Silicon Catalyst, the world's only incubator focused exclusively on accelerating solutions in silicon. Silicon Catalyst, named UBM/Canon's Startup Company of the Year, is now in its fifth year of operations and has engaged with over 300 startups.

What makes Silicon Catalyst Angels unique is not only our visibility into an exclusive deal flow pipeline, but our membership is comprised of seasoned semiconductor veterans who bring with them a wealth of knowledge along with their ability to invest. Driven by passion and a desire to 'give back', our members understand the hardware space thanks to a lifetime of engagement in the industry. When you couple our members enthusiasm, knowledge, and broad network of connections with companies that have been vetted and admitted to Silicon Catalyst, you have a formula that is to date, non existent within the investment community.

The Angel group is wrapping up it's first year of operation and has participated in funding for 5 companies from the Silicon Catalyst Incubator, with total investment amount in excess of $750,000:

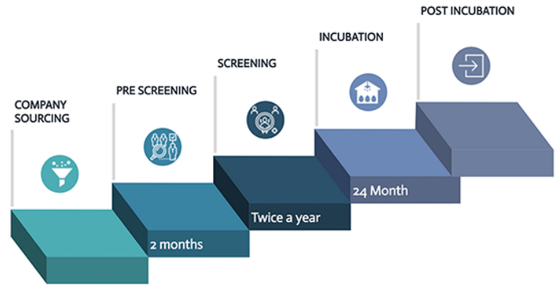
- Owl Autonomous Imaging
- Eridan Communications
- Espre Technologies
- Dover Microsystems
- Mentium



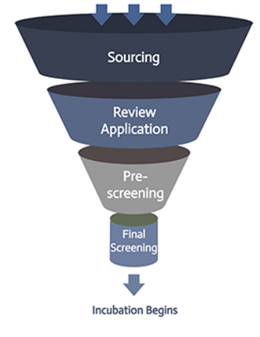
Accredited investors interested in learning more about the Angel group can contact Richard Curtin for membership information – richard@siliconcatalystangels.com

www.siliconcatalystangels.com

The Silicon Catalyst Process™



INCUBATOR SELECTION PROCESS



SOURCING
Companies are sourced from Silicon Catalyst Ecosystem.

REVIEW APPLICATION
Companies apply to Silicon Catalyst via Proseeder.

PRESCREENING
Silicon Catalyst ecosystem members will review companies.

Final SCREENING
A larger group of ecosystem members will review applicants to determine best fit for Silicon Catalyst Incubator admission.

24-MONTH INCUBATION

BEGINNING OF INCUBATION
Develop a customized 24 month incubation plan covering the following:

Advocate and Advisor engagement

Product Planning and In-Kind services connection to support product development

Product Market Fit

Operational Planning

Fundraising Plan

DURING INCUBATION
Regular interaction with a dedicated Silicon Catalyst advocate and advisor

Development of comprehensive fundraising Deck

Periodic Status Update to ecosystem

Assist with staffing

Connect with In-Kind Partners

Connect with investors

Connect with Strategic Partners

INCUBATOR CURRICULUM

PROBLEM/SOLUTION
Clearly articulate Problem or opportunity.
Define your solution

GO TO MARKET
How to target and reach your customer
Customer traction
Sales

TEAM
Building a credible and capable team

MARKETING OPPORTUNITY
Market opportunity
Potential Customers
Competition

LEGAL
Corporate
Intellectual Property

FINANCIAL
Create financial plan
Create funding timeline to support plan

The Silicon Catalyst Team

Rick Lazansky
Chairman,
Co-Founder,
C?O

Pete Rodriguez
CEO

Nick Kepler
COO

Tarun Verma
Managing Partner

Richard Curtin
Managing Partner

Paul Pickering
Managing Partner

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